SSD1789A

Advance Information

132 RGB x 132 CSTN
LCD Segment / Common COLOR Driver with Controller

SOLOMON SYSTECH

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1 GENERAL DESCRIPTION

SSD1789A is a single-chip CMOS color STN LCD driver with controller for dot-matrix graphic liquid crystal display system. SSD1789A consists of 528 high voltage driving output pins for driving maximum 132 RGB Segments, 132 Commons CSTN panel.

SSD1789A consists of 132 RGB x 132 x 18 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through 16-bit/8-bit 6800-series / 8080-series compatible Parallel Interface or 3-wires / 4-wires Serial Peripheral Interface by pins selection.

SSD1789A embeds On-Chip Oscillator, DC-DC Converter, bias divider so as to reduce the number of external component. With the advanced design, low power consumption, stable LCD operating voltage and flexible die package layout, SSD1789A is suitable for any portable battery-driven applications requiring long operation period with compact size.

2 FEATURES

- Power Supply: V_{DDIO} = 1.2V – V_{DD}
  V_{DD} = 2.4V – 3.6V
  V_{CI} = V_{DD} – 3.6V
- LCD Driving Output Voltage: 16V max
- Low Current Sleep Mode
- Maximum display size: 132 RGB columns by 132 rows.
- Display color support: 262K/65K/4K/256 color selectable, with preset/programmable color look up table (CLUT)
- 16-bit/8-bit 6800-series Parallel Interface, 16-bit/8-bit 8080-series Parallel Interface, 3-wires Serial Peripheral Interface and 4-wires Serial Peripheral Interface
- On-Chip (132 RGB) X (132) x 18 = 313632 bits Graphic Display Data RAM
- Programmable partial display function
- Column Re-mapping and RAM Page scan direction control
- Software selection on Center Screen Scrolling, Top Screen Scrolling, Bottom Screen Scrolling and Whole Screen Scrolling
- On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
- 4X / 5X / 6X/ 7X On-Chip DC-DC Converter
- 64 Levels Internal Contrast Control
- Programmable LCD Driving Voltage Temperature Compensation Coefficients
- On-Chip Bias Divider
- Programmable drive duty ratio: 1/32 to 1 /132
- On-Chip Oscillator
- Non-Volatile Memory (OTP) for calibration
- On-Chip 2-D Graphic Acceleration Engine featuring Line/Rectangle Drawing, Dim/Clear/Copy operation in Window mode.
- FRC or PWM Driving Scheme
- Interlace/progressive LCD common pins sequence selectable

3 ORDERING INFORMATION

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1789AZ	132x3 (396)	132	Gold Bump Die	Figure 2 on page 8	

Table 1 - Ordering Information

4 BLOCK DIAGRAM

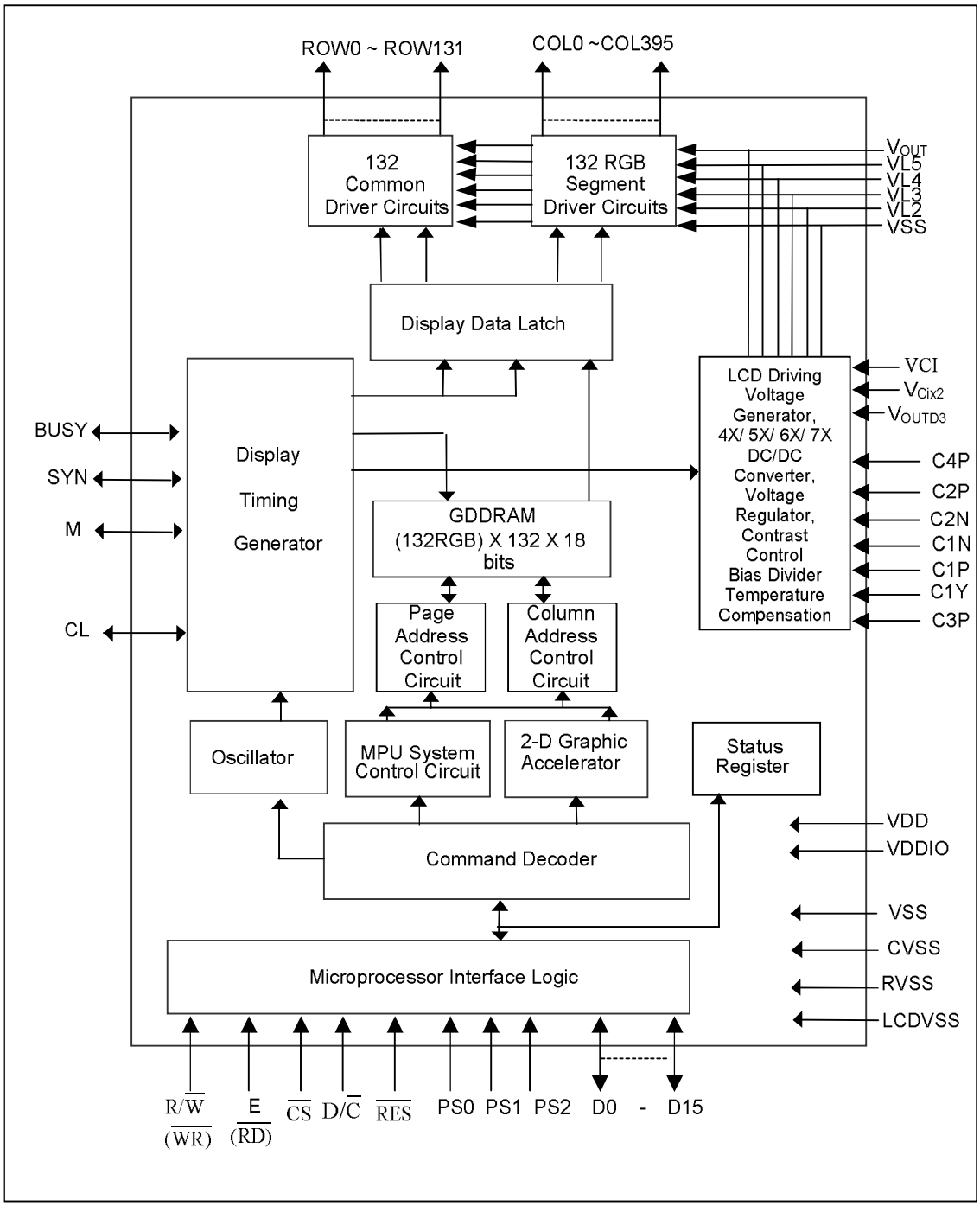
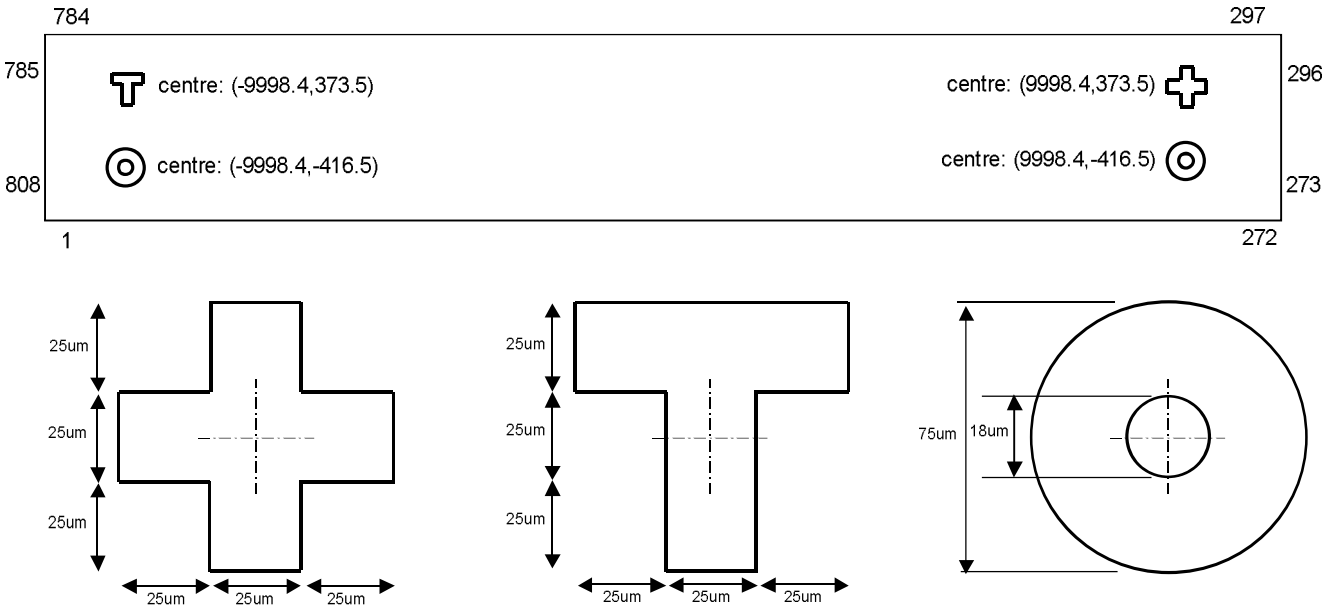


Figure 1 - SSD1789A Block Diagram

5 DIE PAD FLOOR PLAN



Note:
1. Diagram showing die face up
2. Coordinates are reference to die centre (in um)
3. All alignment keys do not contain gold bump

Die size: 20.99 x 1.78 mm^2
Die thickness: 457 +/- 25 um
Bump height: 15um (normal)
Bump co-planarity: <3um (within die)

Bump size:

PAD #	x (um)	y (um)
1-272	56	92
273	118	50
274-295	118	27
296	118	50
297-298	50	118
299-782	27	118
783-784	50	118
785	118	50
786-807	118	27
808	118	50

Figure 2 - SSD1789A Die Pad Floor Plan

Table 2 - SSD1789A Series Bump Die Pad Coordinates (Bump center)

Pad no.	Signal	x coor	y coor	Pad no.	Signal	x coor	y coor	Pad no.	Signal	x coor	y coor
1	DUMMY	-10340.80	-733.00	51	C1Y	-6523.65	-733.00	101	VOUT	-2708.65	-733.00
2	DUMMY	-10262.35	-733.00	52	C1Y	-6447.35	-733.00	102	VOUT	-2632.35	-733.00
3	DUMMY	-10186.05	-733.00	53	C1Y	-6371.05	-733.00	103	VOUT	-2556.05	-733.00
4	C4P	-10109.75	-733.00	54	C1Y	-6294.75	-733.00	104	VOUT	-2479.75	-733.00
5	C4P	-10033.45	-733.00	55	C1Y	-6218.45	-733.00	105	NC	-2403.45	-733.00
6	C4P	-9957.15	-733.00	56	C1Y	-6142.15	-733.00	106	NC	-2327.15	-733.00
7	C4P	-9880.85	-733.00	57	C1Y	-6065.85	-733.00	107	NC	-2250.85	-733.00
8	C4P	-9804.55	-733.00	58	C3P	-5989.55	-733.00	108	NC	-2174.55	-733.00
9	C4P	-9728.25	-733.00	59	C3P	-5913.25	-733.00	109	M	-2098.25	-733.00
10	C4P	-9651.95	-733.00	60	C3P	-5836.95	-733.00	110	SYN	-2021.95	-733.00
11	C2P	-9575.65	-733.00	61	C3P	-5760.65	-733.00	111	CL	-1945.65	-733.00
12	C2P	-9499.35	-733.00	62	C3P	-5684.35	-733.00	112	$\overline{RES}$	-1869.35	-733.00
13	C2P	-9423.05	-733.00	63	C3P	-5608.05	-733.00	113	D/$\overline{C}$	-1793.05	-733.00
14	C2P	-9346.75	-733.00	64	C3P	-5531.75	-733.00	114	D/$\overline{C}$	-1716.75	-733.00
15	C2P	-9270.45	-733.00	65	C3P	-5455.45	-733.00	115	D/$\overline{C}$	-1640.45	-733.00
16	C2P	-9194.15	-733.00	66	NC	-5379.15	-733.00	116	$\overline{CS}$	-1564.15	-733.00
17	C2P	-9117.85	-733.00	67	NC	-5302.85	-733.00	117	$\overline{CS}$	-1487.85	-733.00
18	C2N	-9041.55	-733.00	68	NC	-5226.55	-733.00	118	VSS	-1411.55	-733.00
19	C2N	-8965.25	-733.00	69	NC	-5150.25	-733.00	119	PS2	-1335.25	-733.00
20	C2N	-8888.95	-733.00	70	NC	-5073.95	-733.00	120	VDD	-1258.95	-733.00
21	C2N	-8812.65	-733.00	71	NC	-4997.65	-733.00	121	PS1	-1182.65	-733.00
22	C2N	-8736.35	-733.00	72	VLREF	-4921.35	-733.00	122	VSS	-1106.35	-733.00
23	C2N	-8660.05	-733.00	73	VOUTD3	-4845.05	-733.00	123	PS0	-1030.05	-733.00
24	C2N	-8583.75	-733.00	74	VOUTD3	-4768.75	-733.00	124	VDD	-953.75	-733.00
25	NC	-8507.45	-733.00	75	VOUTD3	-4692.45	-733.00	125	VSS	-877.45	-733.00
26	NC	-8431.15	-733.00	76	VOUTD3	-4616.15	-733.00	126	R/$\overline{W}$ ($\overline{WR}$)	-801.15	-733.00
27	NC	-8354.85	-733.00	77	VOUTD3	-4539.85	-733.00	127	R/$\overline{W}$ ($\overline{WR}$)	-724.85	-733.00
28	NC	-8278.55	-733.00	78	VOUTD3	-4463.55	-733.00	128	E ($\overline{RD}$)	-648.55	-733.00
29	NC	-8202.25	-733.00	79	VOUTD3	-4387.25	-733.00	129	E ($\overline{RD}$)	-572.25	-733.00
30	C1N	-8125.95	-733.00	80	VOUTD3	-4310.95	-733.00	130	VDD	-495.95	-733.00
31	C1N	-8049.65	-733.00	81	VOUTD3	-4234.65	-733.00	131	D0	-419.65	-733.00
32	C1N	-7973.35	-733.00	82	VOUTD3	-4158.35	-733.00	132	D1	-343.35	-733.00
33	C1N	-7897.05	-733.00	83	VOUTD3	-4082.05	-733.00	133	D2	-267.05	-733.00
34	C1N	-7820.75	-733.00	84	VOUTD3	-4005.75	-733.00	134	D3	-190.75	-733.00
35	C1N	-7744.45	-733.00	85	VSS	-3929.45	-733.00	135	D4	-114.45	-733.00
36	C1N	-7668.15	-733.00	86	VSS	-3853.15	-733.00	136	D5	-38.15	-733.00
37	C1N	-7591.85	-733.00	87	VSS	-3776.85	-733.00	137	D6	38.15	-733.00
38	C1P	-7515.55	-733.00	88	VSS	-3700.55	-733.00	138	D7	114.45	-733.00
39	C1P	-7439.25	-733.00	89	VSS	-3624.25	-733.00	139	D8	190.75	-733.00
40	C1P	-7362.95	-733.00	90	VOUT	-3547.95	-733.00	140	D9	267.05	-733.00
41	C1P	-7286.65	-733.00	91	VOUT	-3471.65	-733.00	141	D10	343.35	-733.00
42	C1P	-7210.35	-733.00	92	VOUT	-3395.35	-733.00	142	D11	419.65	-733.00
43	C1P	-7134.05	-733.00	93	VOUT	-3319.05	-733.00	143	D12	495.95	-733.00
44	C1P	-7057.75	-733.00	94	VOUT	-3242.75	-733.00	144	D13	572.25	-733.00
45	C1P	-6981.45	-733.00	95	VOUT	-3166.45	-733.00	145	D14	648.55	-733.00
46	VSS	-6905.15	-733.00	96	VOUT	-3090.15	-733.00	146	D15	724.85	-733.00
47	NC	-6828.85	-733.00	97	VOUT	-3013.85	-733.00	147	BUSY	801.15	-733.00
48	NC	-6752.55	-733.00	98	VOUT	-2937.55	-733.00	148	NC	877.45	-733.00
49	NC	-6676.25	-733.00	99	VOUT	-2861.25	-733.00	149	NC	953.75	-733.00
50	C1Y	-6599.95	-733.00	100	VOUT	-2784.95	-733.00	150	NC	1030.05	-733.00

Pad no.	Signal	x coor	y coor	Pad no.	Signal	x coor	y coor	Pad no.	Signal	x coor	y coor
151	RVSS	1106.35	-733.00	201	VDD	4921.35	-733.00	251	VL2	8736.35	-733.00
152	CVSS	1182.65	-733.00	202	VDD	4997.65	-733.00	252	VL3	8812.65	-733.00
153	CVSS	1258.95	-733.00	203	VDD	5073.95	-733.00	253	VL3	8888.95	-733.00
154	CVSS	1335.25	-733.00	204	VDD	5150.25	-733.00	254	VL3	8965.25	-733.00
155	CVSS	1411.55	-733.00	205	VDD	5226.55	-733.00	255	VL3	9041.55	-733.00
156	CVSS	1487.85	-733.00	206	VDD	5302.85	-733.00	256	VL3	9117.85	-733.00
157	CVSS	1564.15	-733.00	207	VDD	5379.15	-733.00	257	VL4	9194.15	-733.00
158	CVSS	1640.45	-733.00	208	VDDIO	5455.45	-733.00	258	VL4	9270.45	-733.00
159	CVSS	1716.75	-733.00	209	VDDIO	5531.75	-733.00	259	VL4	9346.75	-733.00
160	CVSS	1793.05	-733.00	210	VCIX2	5608.05	-733.00	260	VL4	9423.05	-733.00
161	CVSS	1869.35	-733.00	211	VCIX2	5684.35	-733.00	261	VL4	9499.35	-733.00
162	VSS	1945.65	-733.00	212	VCIX2	5760.65	-733.00	262	VL4	9575.65	-733.00
163	VSS	2021.95	-733.00	213	VCIX2	5836.95	-733.00	263	VL4	9651.95	-733.00
164	VSS	2098.25	-733.00	214	VCIX2	5913.25	-733.00	264	VL5	9728.25	-733.00
165	VSS	2174.55	-733.00	215	VCIX2	5989.55	-733.00	265	VL5	9804.55	-733.00
166	VSS	2250.85	-733.00	216	VCIX2	6065.85	-733.00	266	VL5	9880.85	-733.00
167	VSS	2327.15	-733.00	217	VCIX2	6142.15	-733.00	267	VL5	9957.15	-733.00
168	VSS	2403.45	-733.00	218	VHREF	6218.45	-733.00	268	VL5	10033.45	-733.00
169	VSS	2479.75	-733.00	219	VOUT	6294.75	-733.00	269	NC	10109.75	-733.00
170	VSS	2556.05	-733.00	220	VLREF	6371.05	-733.00	270	DUMMY	10186.05	-733.00
171	VSS	2632.35	-733.00	221	VCI	6447.35	-733.00	271	DUMMY	10262.35	-733.00
172	VSS	2708.65	-733.00	222	VCI	6523.65	-733.00	272	DUMMY	10340.80	-733.00
173	VSS	2784.95	-733.00	223	VCI	6599.95	-733.00				
174	LCDVSS	2861.25	-733.00	224	VCI	6676.25	-733.00				
175	LCDVSS	2937.55	-733.00	225	VCI	6752.55	-733.00				
176	LCDVSS	3013.85	-733.00	226	VCI	6828.85	-733.00				
177	LCDVSS	3090.15	-733.00	227	VCI	6905.15	-733.00				
178	LCDVSS	3166.45	-733.00	228	VCI	6981.45	-733.00				
179	LCDVSS	3242.75	-733.00	229	VCI	7057.75	-733.00				
180	LCDVSS	3319.05	-733.00	230	VCI	7134.05	-733.00				
181	LCDVSS	3395.35	-733.00	231	NC	7210.35	-733.00				
182	LCDVSS	3471.65	-733.00	232	NC	7286.65	-733.00				
183	LCDVSS	3547.95	-733.00	233	NC	7362.95	-733.00				
184	LCDVSS	3624.25	-733.00	234	NC	7439.25	-733.00				
185	LCDVSS	3700.55	-733.00	235	NC	7515.55	-733.00				
186	LCDVSS	3776.85	-733.00	236	NC	7591.85	-733.00				
187	LCDVSS	3853.15	-733.00	237	NC	7668.15	-733.00				
188	LCDVSS	3929.45	-733.00	238	NC	7744.45	-733.00				
189	VDD	4005.75	-733.00	239	VSS	7820.75	-733.00				
190	VDD	4082.05	-733.00	240	VSS	7897.05	-733.00				
191	VDD	4158.35	-733.00	241	VSS	7973.35	-733.00				
192	VDD	4234.65	-733.00	242	VSS	8049.65	-733.00				
193	VDD	4310.95	-733.00	243	VSS	8125.95	-733.00				
194	VDD	4387.25	-733.00	244	VLREF	8202.25	-733.00				
195	VDD	4463.55	-733.00	245	VCIX2	8278.55	-733.00				
196	VDD	4539.85	-733.00	246	VL3	8354.85	-733.00				
197	VDD	4616.15	-733.00	247	VL2	8431.15	-733.00				
198	VDD	4692.45	-733.00	248	VL2	8507.45	-733.00				
199	VDD	4768.75	-733.00	249	VL2	8583.75	-733.00				
200	VDD	4845.05	-733.00	250	VL2	8660.05	-733.00				

Pad no.	Name	x coor	y coor
273	DUMMY	10310.80	-526.60
274	ROW0	10310.80	-473.30
275	ROW1	10310.80	-431.50
276	ROW2	10310.80	-389.70
277	ROW3	10310.80	-347.90
278	ROW4	10310.80	-306.10
279	ROW5	10310.80	-264.30
280	ROW6	10310.80	-222.50
281	ROW7	10310.80	-180.70
282	ROW8	10310.80	-138.90
283	ROW9	10310.80	-97.10
284	ROW10	10310.80	-55.30
285	ROW11	10310.80	-13.50
286	ROW12	10310.80	28.30
287	ROW13	10310.80	70.10
288	ROW14	10310.80	111.90
289	ROW15	10310.80	153.70
290	ROW16	10310.80	195.50
291	ROW17	10310.80	237.30
292	ROW18	10310.80	279.10
293	ROW19	10310.80	320.90
294	ROW20	10310.80	362.70
295	ROW21	10310.80	404.50
296	DUMMY	10310.80	457.80
297	DUMMY	10344.80	706.00
298	DUMMY	10231.60	706.00
299	ROW22	10178.30	706.00
300	ROW23	10136.50	706.00
301	ROW24	10094.70	706.00
302	ROW25	10052.90	706.00
303	ROW26	10011.10	706.00
304	ROW27	9969.30	706.00
305	ROW28	9927.50	706.00
306	ROW29	9885.70	706.00
307	ROW30	9843.90	706.00
308	ROW31	9802.10	706.00
309	ROW32	9760.30	706.00
310	ROW33	9718.50	706.00
311	ROW34	9676.70	706.00
312	ROW35	9634.90	706.00
313	ROW36	9593.10	706.00
314	ROW37	9551.30	706.00
315	ROW38	9509.50	706.00
316	ROW39	9467.70	706.00
317	ROW40	9425.90	706.00
318	ROW41	9384.10	706.00
319	ROW42	9342.30	706.00
320	ROW43	9300.50	706.00
321	ROW44	9258.70	706.00
322	ROW45	9216.90	706.00

Pad no.	Name	x coor	y coor
323	ROW46	9175.10	706.00
324	ROW47	9133.30	706.00
325	ROW48	9091.50	706.00
326	ROW49	9049.70	706.00
327	ROW50	9007.90	706.00
328	ROW51	8966.10	706.00
329	ROW52	8924.30	706.00
330	ROW53	8882.50	706.00
331	ROW54	8840.70	706.00
332	ROW55	8798.90	706.00
333	ROW56	8757.10	706.00
334	ROW57	8715.30	706.00
335	ROW58	8673.50	706.00
336	ROW59	8631.70	706.00
337	ROW60	8589.90	706.00
338	ROW61	8548.10	706.00
339	ROW62	8506.30	706.00
340	ROW63	8464.50	706.00
341	ROW64	8422.70	706.00
342	ROW65	8380.90	706.00

Pad no.	Name	Signal	Color	x coor	y coor
343	COL395	SEG131	B	8255.50	706.00
344	COL394		G	8213.70	706.00
345	COL393		R	8171.90	706.00
346	COL392	SEG130	B	8130.10	706.00
347	COL391		G	8088.30	706.00
348	COL390		R	8046.50	706.00
349	COL389	SEG129	B	8004.70	706.00
350	COL388		G	7962.90	706.00
351	COL387		R	7921.10	706.00
352	COL386	SEG128	B	7879.30	706.00
353	COL385		G	7837.50	706.00
354	COL384		R	7795.70	706.00
355	COL383	SEG127	B	7753.90	706.00
356	COL382		G	7712.10	706.00
357	COL381		R	7670.30	706.00
358	COL380	SEG126	B	7628.50	706.00
359	COL379		G	7586.70	706.00
360	COL378		R	7544.90	706.00
361	COL377	SEG125	B	7503.10	706.00
362	COL376		G	7461.30	706.00
363	COL375		R	7419.50	706.00
364	COL374	SEG124	B	7377.70	706.00
365	COL373		G	7335.90	706.00
366	COL372		R	7294.10	706.00
367	COL371	SEG123	B	7252.30	706.00
368	COL370		G	7210.50	706.00
369	COL369		R	7168.70	706.00
370	COL368	SEG122	B	7126.90	706.00
371	COL367		G	7085.10	706.00
372	COL366		R	7043.30	706.00
373	COL365	SEG121	B	7001.50	706.00
374	COL364		G	6959.70	706.00
375	COL363		R	6917.90	706.00
376	COL362	SEG120	B	6876.10	706.00
377	COL361		G	6834.30	706.00
378	COL360		R	6792.50	706.00
379	COL359	SEG119	B	6750.70	706.00
380	COL358		G	6708.90	706.00
381	COL357		R	6667.10	706.00
382	COL356	SEG118	B	6625.30	706.00
383	COL355		G	6583.50	706.00
384	COL354		R	6541.70	706.00
385	COL353	SEG117	B	6499.90	706.00
386	COL352		G	6458.10	706.00
387	COL351		R	6416.30	706.00
388	COL350	SEG116	B	6374.50	706.00
389	COL349		G	6332.70	706.00
390	COL348		R	6290.90	706.00
391	COL347	SEG115	B	6249.10	706.00
392	COL346		G	6207.30	706.00
393	COL345		R	6165.50	706.00

Pad no.	Name	Signal	Color	x coor	y coor	Pad no.	Name	Signal	Color	x coor	y coor
394	COL344	SEG114	B	6123.70	706.00	445	COL293	SEG97	B	3991.90	706.00
395	COL343		G	6081.90	706.00	446	COL292		G	3950.10	706.00
396	COL342		R	6040.10	706.00	447	COL291		R	3908.30	706.00
397	COL341	SEG113	B	5998.30	706.00	448	COL290	SEG96	B	3866.50	706.00
398	COL340		G	5956.50	706.00	449	COL289		G	3824.70	706.00
399	COL339		R	5914.70	706.00	450	COL288		R	3782.90	706.00
400	COL338	SEG112	B	5872.90	706.00	451	COL287	SEG95	B	3741.10	706.00
401	COL337		G	5831.10	706.00	452	COL286		G	3699.30	706.00
402	COL336		R	5789.30	706.00	453	COL285		R	3657.50	706.00
403	COL335	SEG111	B	5747.50	706.00	454	COL284	SEG94	B	3615.70	706.00
404	COL334		G	5705.70	706.00	455	COL283		G	3573.90	706.00
405	COL333		R	5663.90	706.00	456	COL282		R	3532.10	706.00
406	COL332	SEG110	B	5622.10	706.00	457	COL281	SEG93	B	3490.30	706.00
407	COL331		G	5580.30	706.00	458	COL280		G	3448.50	706.00
408	COL330		R	5538.50	706.00	459	COL279		R	3406.70	706.00
409	COL329	SEG109	B	5496.70	706.00	460	COL278	SEG92	B	3364.90	706.00
410	COL328		G	5454.90	706.00	461	COL277		G	3323.10	706.00
411	COL327		R	5413.10	706.00	462	COL276		R	3281.30	706.00
412	COL326	SEG108	B	5371.30	706.00	463	COL275	SEG91	B	3239.50	706.00
413	COL325		G	5329.50	706.00	464	COL274		G	3197.70	706.00
414	COL324		R	5287.70	706.00	465	COL273		R	3155.90	706.00
415	COL323	SEG107	B	5245.90	706.00	466	COL272	SEG90	B	3114.10	706.00
416	COL322		G	5204.10	706.00	467	COL271		G	3072.30	706.00
417	COL321		R	5162.30	706.00	468	COL270		R	3030.50	706.00
418	COL320	SEG106	B	5120.50	706.00	469	COL269	SEG89	B	2988.70	706.00
419	COL319		G	5078.70	706.00	470	COL268		G	2946.90	706.00
420	COL318		R	5036.90	706.00	471	COL267		R	2905.10	706.00
421	COL317	SEG105	B	4995.10	706.00	472	COL266	SEG88	B	2863.30	706.00
422	COL316		G	4953.30	706.00	473	COL265		G	2821.50	706.00
423	COL315		R	4911.50	706.00	474	COL264		R	2779.70	706.00
424	COL314	SEG104	B	4869.70	706.00	475	COL263	SEG87	B	2737.90	706.00
425	COL313		G	4827.90	706.00	476	COL262		G	2696.10	706.00
426	COL312		R	4786.10	706.00	477	COL261		R	2654.30	706.00
427	COL311	SEG103	B	4744.30	706.00	478	COL260	SEG86	B	2612.50	706.00
428	COL310		G	4702.50	706.00	479	COL259		G	2570.70	706.00
429	COL309		R	4660.70	706.00	480	COL258		R	2528.90	706.00
430	COL308	SEG102	B	4618.90	706.00	481	COL257	SEG85	B	2487.10	706.00
431	COL307		G	4577.10	706.00	482	COL256		G	2445.30	706.00
432	COL306		R	4535.30	706.00	483	COL255		R	2403.50	706.00
433	COL305	SEG101	B	4493.50	706.00	484	COL254	SEG84	B	2361.70	706.00
434	COL304		G	4451.70	706.00	485	COL253		G	2319.90	706.00
435	COL303		R	4409.90	706.00	486	COL252		R	2278.10	706.00
436	COL302	SEG100	B	4368.10	706.00	487	COL251	SEG83	B	2236.30	706.00
437	COL301		G	4326.30	706.00	488	COL250		G	2194.50	706.00
438	COL300		R	4284.50	706.00	489	COL249		R	2152.70	706.00
439	COL299	SEG99	B	4242.70	706.00	490	COL248	SEG82	B	2110.90	706.00
440	COL298		G	4200.90	706.00	491	COL247		G	2069.10	706.00
441	COL297		R	4159.10	706.00	492	COL246		R	2027.30	706.00
442	COL296	SEG98	B	4117.30	706.00	493	COL245	SEG81	B	1985.50	706.00
443	COL295		G	4075.50	706.00	494	COL244		G	1943.70	706.00
444	COL294		R	4033.70	706.00	495	COL243		R	1901.90	706.00

Pad no.	Name	Signal	Color	x coor	y coor	Pad no.	Name	Signal	Color	x coor	y coor
496	COL242		B	1860.10	706.00	547	COL191		B	-271.70	706.00
497	COL241	SEG80	G	1818.30	706.00	548	COL190	SEG63	G	-313.50	706.00
498	COL240		R	1776.50	706.00	549	COL189		R	-355.30	706.00
499	COL239		B	1734.70	706.00	550	COL188		B	-397.10	706.00
500	COL238	SEG79	G	1692.90	706.00	551	COL187	SEG62	G	-438.90	706.00
501	COL237		R	1651.10	706.00	552	COL186		R	-480.70	706.00
502	COL236		B	1609.30	706.00	553	COL185		B	-522.50	706.00
503	COL235	SEG78	G	1567.50	706.00	554	COL184	SEG61	G	-564.30	706.00
504	COL234		R	1525.70	706.00	555	COL183		R	-606.10	706.00
505	COL233		B	1483.90	706.00	556	COL182		B	-647.90	706.00
506	COL232	SEG77	G	1442.10	706.00	557	COL181	SEG60	G	-689.70	706.00
507	COL231		R	1400.30	706.00	558	COL180		R	-731.50	706.00
508	COL230		B	1358.50	706.00	559	COL179		B	-773.30	706.00
509	COL229	SEG76	G	1316.70	706.00	560	COL178	SEG59	G	-815.10	706.00
510	COL228		R	1274.90	706.00	561	COL177		R	-856.90	706.00
511	COL227		B	1233.10	706.00	562	COL176		B	-898.70	706.00
512	COL226	SEG75	G	1191.30	706.00	563	COL175	SEG58	G	-940.50	706.00
513	COL225		R	1149.50	706.00	564	COL174		R	-982.30	706.00
514	COL224		B	1107.70	706.00	565	COL173		B	-1024.10	706.00
515	COL223	SEG74	G	1065.90	706.00	566	COL172	SEG57	G	-1065.90	706.00
516	COL222		R	1024.10	706.00	567	COL171		R	-1107.70	706.00
517	COL221		B	982.30	706.00	568	COL170		B	-1149.50	706.00
518	COL220	SEG73	G	940.50	706.00	569	COL169	SEG56	G	-1191.30	706.00
519	COL219		R	898.70	706.00	570	COL168		R	-1233.10	706.00
520	COL218		B	856.90	706.00	571	COL167		B	-1274.90	706.00
521	COL217	SEG72	G	815.10	706.00	572	COL166	SEG55	G	-1316.70	706.00
522	COL216		R	773.30	706.00	573	COL165		R	-1358.50	706.00
523	COL215		B	731.50	706.00	574	COL164		B	-1400.30	706.00
524	COL214	SEG71	G	689.70	706.00	575	COL163	SEG54	G	-1442.10	706.00
525	COL213		R	647.90	706.00	576	COL162		R	-1483.90	706.00
526	COL212		B	606.10	706.00	577	COL161		B	-1525.70	706.00
527	COL211	SEG70	G	564.30	706.00	578	COL160	SEG53	G	-1567.50	706.00
528	COL210		R	522.50	706.00	579	COL159		R	-1609.30	706.00
529	COL209		B	480.70	706.00	580	COL158		B	-1651.10	706.00
530	COL208	SEG69	G	438.90	706.00	581	COL157	SEG52	G	-1692.90	706.00
531	COL207		R	397.10	706.00	582	COL156		R	-1734.70	706.00
532	COL206		B	355.30	706.00	583	COL155		B	-1776.50	706.00
533	COL205	SEG68	G	313.50	706.00	584	COL154	SEG51	G	-1818.30	706.00
534	COL204		R	271.70	706.00	585	COL153		R	-1860.10	706.00
535	COL203		B	229.90	706.00	586	COL152		B	-1901.90	706.00
536	COL202	SEG67	G	188.10	706.00	587	COL151	SEG50	G	-1943.70	706.00
537	COL201		R	146.30	706.00	588	COL150		R	-1985.50	706.00
538	COL200		B	104.50	706.00	589	COL149		B	-2027.30	706.00
539	COL199	SEG66	G	62.70	706.00	590	COL148	SEG49	G	-2069.10	706.00
540	COL198		R	20.90	706.00	591	COL147		R	-2110.90	706.00
541	COL197		B	-20.90	706.00	592	COL146		B	-2152.70	706.00
542	COL196	SEG65	G	-62.70	706.00	593	COL145	SEG48	G	-2194.50	706.00
543	COL195		R	-104.50	706.00	594	COL144		R	-2236.30	706.00
544	COL194		B	-146.30	706.00	595	COL143		B	-2278.10	706.00
545	COL193	SEG64	G	-188.10	706.00	596	COL142	SEG47	G	-2319.90	706.00
546	COL192		R	-229.90	706.00	597	COL141		R	-2361.70	706.00

Pad no.	Name	Signal	Color	x coor	y coor	Pad no.	Name	Signal	Color	x coor	y coor
598	COL140		B	-2403.50	706.00	649	COL89		B	-4535.30	706.00
599	COL139	SEG46	G	-2445.30	706.00	650	COL88	SEG29	G	-4577.10	706.00
600	COL138		R	-2487.10	706.00	651	COL87		R	-4618.90	706.00
601	COL137		B	-2528.90	706.00	652	COL86		B	-4660.70	706.00
602	COL136	SEG45	G	-2570.70	706.00	653	COL85	SEG28	G	-4702.50	706.00
603	COL135		R	-2612.50	706.00	654	COL84		R	-4744.30	706.00
604	COL134		B	-2654.30	706.00	655	COL83		B	-4786.10	706.00
605	COL133	SEG44	G	-2696.10	706.00	656	COL82	SEG27	G	-4827.90	706.00
606	COL132		R	-2737.90	706.00	657	COL81		R	-4869.70	706.00
607	COL131		B	-2779.70	706.00	658	COL80		B	-4911.50	706.00
608	COL130	SEG43	G	-2821.50	706.00	659	COL79	SEG26	G	-4953.30	706.00
609	COL129		R	-2863.30	706.00	660	COL78		R	-4995.10	706.00
610	COL128		B	-2905.10	706.00	661	COL77		B	-5036.90	706.00
611	COL127	SEG42	G	-2946.90	706.00	662	COL76	SEG25	G	-5078.70	706.00
612	COL126		R	-2988.70	706.00	663	COL75		R	-5120.50	706.00
613	COL125		B	-3030.50	706.00	664	COL74		B	-5162.30	706.00
614	COL124	SEG41	G	-3072.30	706.00	665	COL73	SEG24	G	-5204.10	706.00
615	COL123		R	-3114.10	706.00	666	COL72		R	-5245.90	706.00
616	COL122		B	-3155.90	706.00	667	COL71		B	-5287.70	706.00
617	COL121	SEG40	G	-3197.70	706.00	668	COL70	SEG23	G	-5329.50	706.00
618	COL120		R	-3239.50	706.00	669	COL69		R	-5371.30	706.00
619	COL119		B	-3281.30	706.00	670	COL68		B	-5413.10	706.00
620	COL118	SEG39	G	-3323.10	706.00	671	COL67	SEG22	G	-5454.90	706.00
621	COL117		R	-3364.90	706.00	672	COL66		R	-5496.70	706.00
622	COL116		B	-3406.70	706.00	673	COL65		B	-5538.50	706.00
623	COL115	SEG38	G	-3448.50	706.00	674	COL64	SEG21	G	-5580.30	706.00
624	COL114		R	-3490.30	706.00	675	COL63		R	-5622.10	706.00
625	COL113		B	-3532.10	706.00	676	COL62		B	-5663.90	706.00
626	COL112	SEG37	G	-3573.90	706.00	677	COL61	SEG20	G	-5705.70	706.00
627	COL111		R	-3615.70	706.00	678	COL60		R	-5747.50	706.00
628	COL110		B	-3657.50	706.00	679	COL59		B	-5789.30	706.00
629	COL109	SEG36	G	-3699.30	706.00	680	COL58	SEG19	G	-5831.10	706.00
630	COL108		R	-3741.10	706.00	681	COL57		R	-5872.90	706.00
631	COL107		B	-3782.90	706.00	682	COL56		B	-5914.70	706.00
632	COL106	SEG35	G	-3824.70	706.00	683	COL55	SEG18	G	-5956.50	706.00
633	COL105		R	-3866.50	706.00	684	COL54		R	-5998.30	706.00
634	COL104		B	-3908.30	706.00	685	COL53		B	-6040.10	706.00
635	COL103	SEG34	G	-3950.10	706.00	686	COL52	SEG17	G	-6081.90	706.00
636	COL102		R	-3991.90	706.00	687	COL51		R	-6123.70	706.00
637	COL101		B	-4033.70	706.00	688	COL50		B	-6165.50	706.00
638	COL100	SEG33	G	-4075.50	706.00	689	COL49	SEG16	G	-6207.30	706.00
639	COL99		R	-4117.30	706.00	690	COL48		R	-6249.10	706.00
640	COL98		B	-4159.10	706.00	691	COL47		B	-6290.90	706.00
641	COL97	SEG32	G	-4200.90	706.00	692	COL46	SEG15	G	-6332.70	706.00
642	COL96		R	-4242.70	706.00	693	COL45		R	-6374.50	706.00
643	COL95		B	-4284.50	706.00	694	COL44		B	-6416.30	706.00
644	COL94	SEG31	G	-4326.30	706.00	695	COL43	SEG14	G	-6458.10	706.00
645	COL93		R	-4368.10	706.00	696	COL42		R	-6499.90	706.00
646	COL92		B	-4409.90	706.00	697	COL41		B	-6541.70	706.00
647	COL91	SEG30	G	-4451.70	706.00	698	COL40	SEG13	G	-6583.50	706.00
648	COL90		R	-4493.50	706.00	699	COL39		R	-6625.30	706.00

Pad no.	Name	Signal	Color	x coor	y coor
700	COL38		B	-6667.10	706.00
701	COL37	SEG12	G	-6708.90	706.00
702	COL36		R	-6750.70	706.00
703	COL35		B	-6792.50	706.00
704	COL34	SEG11	G	-6834.30	706.00
705	COL33		R	-6876.10	706.00
706	COL32		B	-6917.90	706.00
707	COL31	SEG10	G	-6959.70	706.00
708	COL30		R	-7001.50	706.00
709	COL29		B	-7043.30	706.00
710	COL28	SEG9	G	-7085.10	706.00
711	COL27		R	-7126.90	706.00
712	COL26		B	-7168.70	706.00
713	COL25	SEG8	G	-7210.50	706.00
714	COL24		R	-7252.30	706.00
715	COL23		B	-7294.10	706.00
716	COL22	SEG7	G	-7335.90	706.00
717	COL21		R	-7377.70	706.00
718	COL20		B	-7419.50	706.00
719	COL19	SEG6	G	-7461.30	706.00
720	COL18		R	-7503.10	706.00
721	COL17		B	-7544.90	706.00
722	COL16	SEG5	G	-7586.70	706.00
723	COL15		R	-7628.50	706.00
724	COL14		B	-7670.30	706.00
725	COL13	SEG4	G	-7712.10	706.00
726	COL12		R	-7753.90	706.00
727	COL11		B	-7795.70	706.00
728	COL10	SEG3	G	-7837.50	706.00
729	COL9		R	-7879.30	706.00
730	COL8		B	-7921.10	706.00
731	COL7	SEG2	G	-7962.90	706.00
732	COL6		R	-8004.70	706.00
733	COL5		B	-8046.50	706.00
734	COL4	SEG1	G	-8088.30	706.00
735	COL3		R	-8130.10	706.00
736	COL2		B	-8171.90	706.00
737	COL1	SEG0	G	-8213.70	706.00
738	COL0		R	-8255.50	706.00

Pad no.	Name	x coor	y coor
739	ROW66	-8380.90	706.00
740	ROW67	-8422.70	706.00
741	ROW68	-8464.50	706.00
742	ROW69	-8506.30	706.00
743	ROW70	-8548.10	706.00
744	ROW71	-8589.90	706.00
745	ROW72	-8631.70	706.00
746	ROW73	-8673.50	706.00
747	ROW74	-8715.30	706.00
748	ROW75	-8757.10	706.00
749	ROW76	-8798.90	706.00
750	ROW77	-8840.70	706.00
751	ROW78	-8882.50	706.00
752	ROW79	-8924.30	706.00
753	ROW80	-8966.10	706.00
754	ROW81	-9007.90	706.00
755	ROW82	-9049.70	706.00
756	ROW83	-9091.50	706.00
757	ROW84	-9133.30	706.00
758	ROW85	-9175.10	706.00
759	ROW86	-9216.90	706.00
760	ROW87	-9258.70	706.00
761	ROW88	-9300.50	706.00
762	ROW89	-9342.30	706.00
763	ROW90	-9384.10	706.00
764	ROW91	-9425.90	706.00
765	ROW92	-9467.70	706.00
766	ROW93	-9509.50	706.00
767	ROW94	-9551.30	706.00
768	ROW95	-9593.10	706.00
769	ROW96	-9634.90	706.00
770	ROW97	-9676.70	706.00
771	ROW98	-9718.50	706.00
772	ROW99	-9760.30	706.00
773	ROW100	-9802.10	706.00
774	ROW101	-9843.90	706.00
775	ROW102	-9885.70	706.00
776	ROW103	-9927.50	706.00
777	ROW104	-9969.30	706.00
778	ROW105	-10011.10	706.00
779	ROW106	-10052.90	706.00
780	ROW107	-10094.70	706.00
781	ROW108	-10136.50	706.00
782	ROW109	-10178.30	706.00
783	DUMMY	-10231.60	706.00
784	DUMMY	-10344.80	706.00
785	DUMMY	-10310.80	457.80
786	ROW110	-10310.80	404.50
787	ROW111	-10310.80	362.70
788	ROW112	-10310.80	320.90

Pad no.	Name	x coor	y coor
789	ROW113	-10310.80	279.10
790	ROW114	-10310.80	237.30
791	ROW115	-10310.80	195.50
792	ROW116	-10310.80	153.70
793	ROW117	-10310.80	111.90
794	ROW118	-10310.80	70.10
795	ROW119	-10310.80	28.30
796	ROW120	-10310.80	-13.50
797	ROW121	-10310.80	-55.30
798	ROW122	-10310.80	-97.10
799	ROW123	-10310.80	-138.90
800	ROW124	-10310.80	-180.70
801	ROW125	-10310.80	-222.50
802	ROW126	-10310.80	-264.30
803	ROW127	-10310.80	-306.10
804	ROW128	-10310.80	-347.90
805	ROW129	-10310.80	-389.70
806	ROW130	-10310.80	-431.50
807	ROW131	-10310.80	-473.30
808	DUMMY	-10310.80	-526.60

6 PIN DESCRIPTION

6.1 $\overline{CS}$

This pin is the chip selection input. The chip is enabled for MCU communication only when $\overline{CS}$ is pulled low.

6.2 $\overline{RES}$

This pin is the reset signal input. Initialization of the chip is started once the reset pin is pulled low. The minimum pulse width for reset sequence is 10us.

6.3 D/$\overline{C}$

This pin is Data/Command control pin. When the pin is pulled high, the input at D7-D0 is treated as display data. When the pin is pulled low, the input at D7-D0 will be transferred to the command register.

6.4 R/$\overline{W}$ ($\overline{WR}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as Read/Write (R/$\overline{W}$) selection input. Read mode will be carried out when this pin is pulled high and write mode when this pin is pulled low.

When 8080 interface mode is selected, this pin is the Write ($\overline{WR}$) control signal input. Data write operation is initiated when this pin is pulled low and the chip is selected.

6.5 E ($\overline{RD}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/ write operation is initiated when this pin is pulled high and the chip is selected.

When 8080 interface mode is selected, this pin is the Read ($\overline{RD}$) control signal input. Data read operation is initiated when this pin is pulled low and the chip is selected.

6.6 PS0 – PS2

These pins are the bus interface mode selection input. Different bus interface can be selected changing the setting of these pins.

PS2	PS1	PS0	MPU Interface
H	H	H	16-bit 8080 parallel interface
H	H	L	8-bit 8080 parallel interface
H	L	L	16-bit 6800 parallel interface
L	H	H	8-bit 6800 parallel interface
L	L	H	3-lines serial peripheral interface (SPI)
L	L	L	4-lines serial peripheral interface (SPI)

Table 3 - Bus interface mode selection by PS2-PS0

Note1: For serial applications, D0 – D5, D8 – D15, R/$\overline{W}$ ($\overline{WR}$), E($\overline{RD}$) are recommended to connect V_{DD}.
Note2: Read back operation is only available in parallel mode

6.7 D0-D15

These pins are the 16-bit bi-directional data bus in parallel interface mode. D15 is the MSB while D_0 is the LSB. When serial mode selected, D7 is the serial data input SDA and D6 is the serial clock input SCK.

6.8 V_{DD}

This pin is the system power supply pin of the logic block.

6.9 V_{DDIO}

This pin is the system power supply pin of IO buffer. Please refer to Figure 26 on Page 67 for connection example.

6.10 V_{CI}

This pin is the reference voltage input for internal DC-DC converter. The DC-DC converter output is equal to the multiple factor (4X, 5X, 6X or 7X) times V_{CI} with respect to V_{SS}. The maximum output voltage will limit by the max. V_{OUT} characteristic.
Note: Voltage at this input pin must be larger than or equal to V_{DD}. ($V_{CI} \geq V_{DD}$)

6.11 V_{CIX2}

This pin is a voltage reference output which is equal to 2x V_{CI}.

6.12 VLREF

This pin is the ground of operation amplifier VL4 and VL5. It should be connected to VOUTD3.

6.13 VHREF

This pin is the power supply pin of the operation amplifier VL3. It should be connected to VCIX2.

6.14 V_{SS}

This pin is the ground of logic.

6.15 RV_{SS}

This pin is the ground of Vref where Vref is the reference voltage of internal regulator.

6.16 CV_{SS}

This pin is the ground of analog.

6.17 $LCDV_{SS}$

This pin is the ground of segment and common output pins.

6.18 V_{OUT}

This is the most positive voltage supply pin of the chip. It is generated by the internal voltage regulator. This voltage level is used for internal referencing only and the voltage level at V_{OUT} pin is not used for driving external circuitry.

6.19 V_{OUTD3}

This pin is a voltage reference output.

6.20 V_{L5}, V_{L4}, V_{L3} and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$

	1 : a bias
V_{L5}	(a-1)/a * V_{OUT}
V_{L4}	(a-2)/a * V_{OUT}
V_{L3}	2/a * V_{OUT}
V_{L2}	1/a * V_{OUT}

Table 4 - $V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$ Relationship

6.21 ROW0 – ROW131

These pins provide the driving signals, COMMON, to the LCD panel.

6.22 COL0 – COL395

These pins provide the LCD driving signals, SEGMENT, to the LCD panel. The Red, Green, Blue colors signal are sent out from the SEGMENT output at the same time. The output voltage level of these pins is V_{DD} during sleep mode or standby mode.

6.23 C1P, C1N, C2P, C2N, C1Y, C3P, C4P

When internal DC-DC voltage converter is used, external capacitor is connected between these pins. Please refer to the system block diagram for external capacitors connection in Figure 5.

6.24 CL

This pin is the system clock I/O. This pin is the external clock input for the device, which is enabled by using extended command. It should be left open under normal operation. The internal oscillator will be used after power on reset.

6.25 M

This pin is used for cascade purpose only. It should be left open under normal operation.

6.26 SYN

This pin is used for cascade purpose only. It should be left open under normal operation.

6.27 BUSY

This pin will be high during RAM buffer read/write operation and during graphic commands executing. System programmer should read this pin (low is ready, high is busy) before sending next RAM buffer related command (e.g. RAM write – 5CH; RAM read – 5DH OR any graphic commands)

6.28 NC

The No connection (NC) pin should NOT be connected to any signal pin nor shorted to other NC pins in application. It should be left open.

6.29 DUMMY

This pin is a floating dummy pin with no internal circuit connection.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Microprocessor Interface Logic

The Microprocessor Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS2, PS1 and PS0 pins. Please refer to the pin descriptions on page 16.

a) MPU Parallel 6800-series Interface

The parallel Interface consists of 16 bi-directional data pins (D15 – D0), R/$\overline{W}$, D/$\overline{C}$, E and $\overline{CS}$. R/$\overline{W}$ input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Figure 17 to Figure 19 for Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

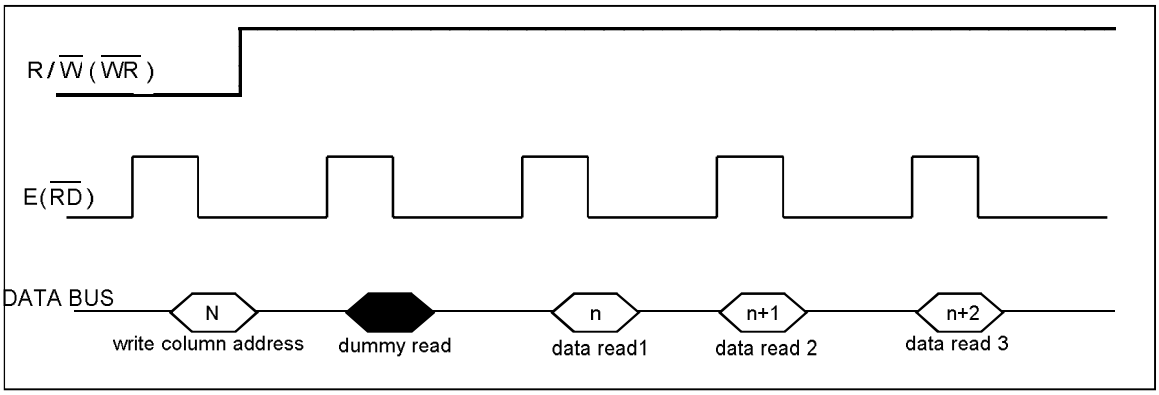


Figure 3 - Read Display Data

b) MPU Parallel 8080-series Interface

The parallel interface consists of 16 bi-directional data pins D_{15} – D_0, $\overline{RD}$, $\overline{WR}$, D/$\overline{C}$ and $\overline{CS}$. $\overline{RD}$ input serves as data read latch signal (clock) when low provided that $\overline{CS}$ is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by D/$\overline{C}$. $\overline{WR}$ input serves as data write latch signal (clock) when low provided that $\overline{CS}$ is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/$\overline{C}$. A dummy read is also required before the first actual display data read for 8080-series interface.

c) MPU 4-lines Serial Peripheral Interface

The 4-lines serial peripheral Interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$ and $\overline{CS}$. SDA is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 …… data bit 0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock. Please refer to Figure 21 & Figure 23 on page 62 & 64 for serial interface timing.

d) MPU 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while $D/\overline{C}$ is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: $D/\overline{C}$ bit, D_7 to D_0 bit. The $D/\overline{C}$ bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM ($D/\overline{C}$ bit = 1) or the command register ($D/\overline{C}$ bit = 0).

	6800 – series Parallel Interface	**8080 – series Parallel Interface**	**3-lines or 4-lines Serial peripheral Interface**
Data Read	16/8-bits	16/8-bits	No
Data Write	16/8-bits	16/8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

Table 5 - Data bus selection modes

7.2 Reset Circuit

This block is integrated into the Microprocessor Interface Logic which includes Power On Reset circuitry and the hardware reset pin, $\overline{RES}$. Both of these having the same reset function. Once the $\overline{RES}$ pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given by:

When $\overline{RES}$ input is low, the chip is initialized to the following:

1.	Display ON/OFF:	Display is OFF
2.	Normal/Inverse Display:	Normal Display
3.	COM Scan Direction:	ROW0-ROW131 = COM0-COM131
4.	Internal Oscillator:	Disable
5.	Reference Voltage Generation Circuit:	Disable
6.	Voltage regulator and Voltage Follower:	Disable
7.	Booster:	Disable
8.	Bias ratio:	1/9
9.	Multiplex ratio:	132 Mux
10.	Contrast level:	20h
11.	Internal Regulator gain:	6.49
12.	Average temperature gradient:	-0.25%/°C
13.	Partial display mode:	Disable
	Start COM address:	0
	End COM address:	0
14.	Area Scroll set	
	Top block address:	0
	Bottom block address:	0
	Number of specified block:	0
	Area scroll mode:	Whole screen scroll mode
15.	Scroll start set	
	Start block address:	0
16.	Data Scan Direction	
	Normal/inverse display of page address:	Normal
	Normal/inverse display of column address:	Normal
	Address-scan direction:	Column direction
	RGB arrangement:	RGB
	Gray-scale setup:	4K color
17.	Start Page Address set:	0
18.	End Page Address set:	0
19.	Start Column address set:	0
20.	End Column address set:	0
21.	Select PWM/FRC	5-bit PWM + 1-bit FRC mode

7.3 Command Decoder

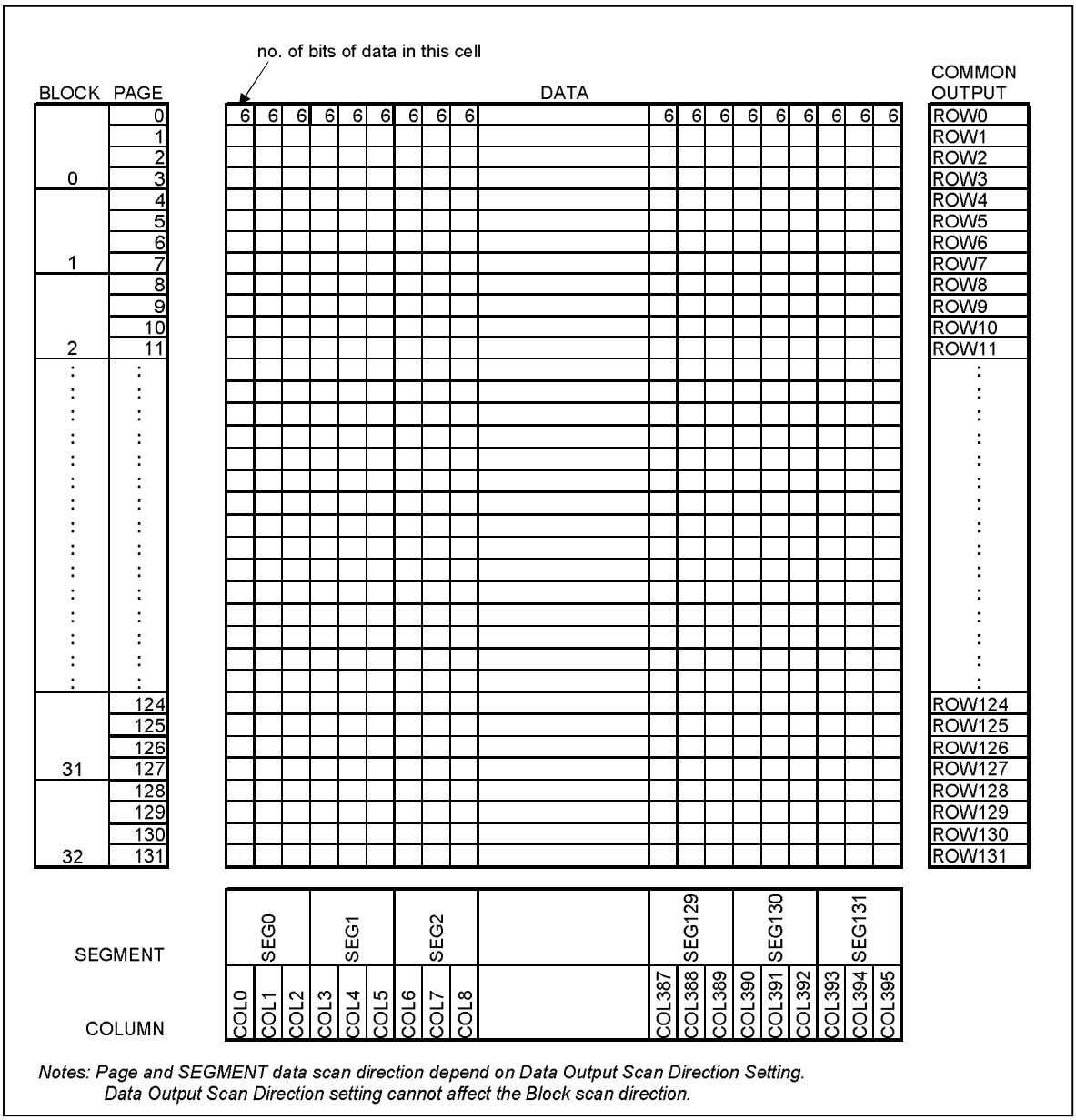
This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ pin is high, data is written to Graphic Display data RAM (GDDRAM). If it is low, the input at D7 – D0 is interpreted as a Command and it will be decoded. The decoded command will be written to the corresponding command register.

7.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 396 (132 RGB) x 132 x 18 = 313632 bits. Figure 4 on page 23 is a description of the GDDRAM address map.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command “Data Output/Scan direction” in Table 6 on page 26 for detail description.

Four pages of display data form a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command “Set area Scroll” and “Set Scroll Start” in Table 13 on page 41.



Notes: Page and SEGMENT data scan direction depend on Data Output Scan Direction Setting.
Data Output Scan Direction setting cannot affect the Block scan direction.

Figure 4 - Graphic Display Data RAM Map

7.5 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of:

1. 4X, 5X, 6X and 7X DC-DC voltage converter
2. Bias Divider - If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{OUT}) to give the LCD driving levels (VL2 – VL5).
3. Contrast Control -Software control of 64 voltage levels of LCD voltage.
4. Bias Ratio Selection circuitry -Software control of 1/7 to 1/10 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry - Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is -0.20%/°C.

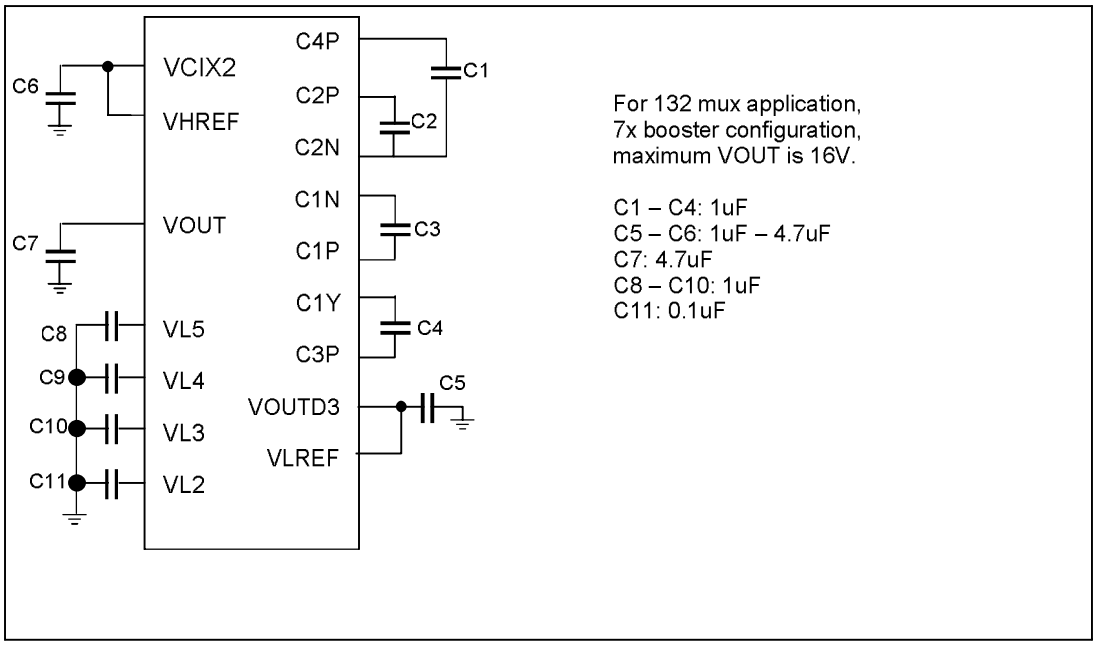


Figure 5 - SSD1789A Booster Configurations

7.6 Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 6). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

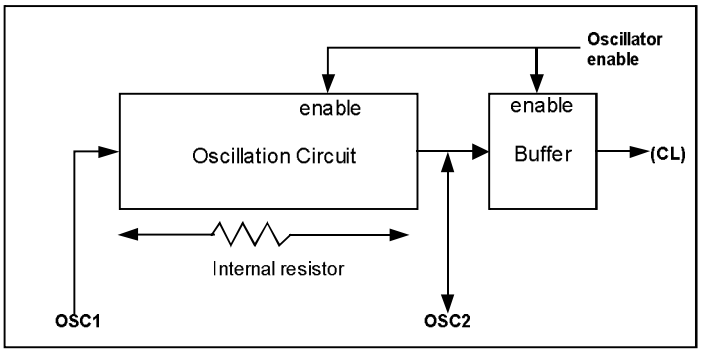


Figure 6 - Oscillator structural block diagram

7.7 Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

7.8 HV Buffer Cell (Level Shifter)

This block is embedded in the Segment/Common Driver Circuits. HV Buffer Cell works as a level shifter, which translates the low voltage output signal to the required driving voltage. The output is shifted out with reference to the internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

7.9 Level Selector

This block is embedded in the Segment/Common Driver circuits. Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

8 COMMAND TABLE

Table 6 - COMMAND TABLE

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	15	0 X_7 Y_7	0 X_6 Y_6	0 X_5 Y_5	1 X_4 Y_4	0 X_3 Y_3	1 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Column Address	Set the start column address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end column address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ Column address = 00000000b (POR) Column address is in a range of 0~131.
0 1 1	75	0 X_7 Y_7	1 X_6 Y_6	1 X_5 Y_5	1 X_4 Y_4	0 X_3 Y_3	1 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Page Address	Set the start page address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end page address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ Page address = 00000000b (POR) Page address is in a range of 0~131.
0 1	BB	1 *	0 *	1 *	1 *	1 *	0 X_2	1 X_1	1 X_0	Set COM Output Scan Direction	X_2 X_1 X_0 ROW0...ROW65 ROW66...ROW131 0 0 0 COM0 ->COM65 COM66 -> COM131 (POR) 0 0 1 COM0 ->COM65 COM131<-COM66 0 1 0 COM65<-COM0 COM66 -> COM131 0 1 1 COM65<-COM0 COM131<-COM66
0 1 1 1	BC	1 * * *	0 * * *	1 * * *	1 * * P_{34}	1 * * P_{33}	1 P_{12} P_{22} P_{32}	0 P_{11} P_{21} P_{31}	0 P_{10} P_{20} P_{30}	Set Data Output Scan Direction	a) Normal or Reverse page/column/scan directions P_{10} = 0: set page address to normal display (POR) P_{10} = 1: set page address to inverse display P_{11} = 0: set column address to normal rotation (POR) P_{11} = 1: set column address to inverse rotation P_{12} = 0: set scan direction to column scan (POR) P_{12} = 1: set scan direction to page scan Please refer to the Figure 7 on page 38 for detail description of column/page scan direction modes b) RGB color arrangement P_{22}, P_{21}, P_{20}: The control bits are used for setting the (RGB) color arrangement of segment output. 000 is the POR value. Please refer to the Table 11 on page 39 for detail mapping of the segment output. c) Gray-scale selection P_{31} P_{30} Gray-scale modes 0 0 16-bit/pixel mode 0 1 8-bit/pixel mode 1 0 12-bit/pixel mode (POR) 1 1 18-bit/pixel mode P_{32} = 0: direct write mode (POR) P_{32} = 1: use gamma correction P_{34} P_{33} 0 0 type A (if using 18-bit/pixel mode) (POR) 0 1 type B (if using 18-bit/pixel mode) 1 0 type C (if using 18-bit/pixel mode) Please refer to the Table 12 on page 40 for detail description of different gray-scale selection modes. Different gray-scale selection modes.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	CE	1	1	0	0	1	1	1	0	Set 262K/65K/4K/256 - Color Look Up Table (LUT)	N=32 for 18 bit mode N=32 for 16 bit mode N=16 for 12 bit mode N=10 for 8 bit mode
1		*	*	X_{51}	X_{41}	X_{31}	X_{21}	X_{11}	X_{01}		
1		*	*	X_{52}	X_{42}	X_{32}	X_{22}	X_{12}	X_{02}		
					:						
					:						
1		*	*	X_{58}	X_{48}	X_{38}	X_{28}	X_{18}	X_{08}		
1		*	*	X_{59}	X_{49}	X_{39}	X_{29}	X_{19}	X_{09}		
					:						
					:						
1		*	*	X_{516}	X_{416}	X_{316}	X_{216}	X_{116}	X_{016}		
1		*	*	X_{517}	X_{417}	X_{317}	X_{217}	X_{117}	X_{017}		
					:						
					:						
1		*	*	X_{5N}	X_{4N}	X_{3N}	X_{2N}	X_{1N}	X_{0N}		
0	CA	1	1	0	0	1	0	1	0	Set Display Control	Driver duty selection Select driver duty from 1/32 to 1/132. As $Y_5\,Y_4\,Y_3\,Y_2\,Y_1\,Y_0$ is increased from 000001b to 100111b, the number of display lines, N is increased at the same rating. To specify the $Y_5\,Y_4\,Y_3\,Y_2\,Y_1\,Y_0$. $Y_5 \sim Y_0 = \frac{N}{4} - 1$
1	0	0	0	0	0	0	0	0	0		
1		*	*	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0		
1	0	0	0	0	0	0	0	0	0		
0	AA	1	0	1	0	1	0	1	0	Set Area Scroll	a) Top Block Address $X_5X_4X_3X_2X_1X_0$ is used to specify the block address (1 block = 4 lines) at the top of the scrolling area. Top block address = 000000b (POR) b) Bottom Block Address $Y_5Y_4Y_3Y_2Y_1Y_0$ is used to specify the block address (1 block = 4 lines) at the bottom of the scrolling area. Bottom block address = 000000b (POR) c) Number of specified Blocks The number of specified blocks = Number of (Top fixed area + Scroll area) blocks –1. If bottom scroll or whole screen scroll mode is chosen, the number of specified blocks is set to Z_5~ Z_0 Number of specified blocks = 000000b (POR) d) Area Scroll Mode There are four types of area scroll. P_{41} P_{40} Types of Area Scroll 0 0 Center Screen Scroll 0 1 Top Screen Scroll 1 0 Bottom Screen Scroll 1 1 Whole Screen Scroll Type of area scroll = Whole Screen Scroll (POR)
1		*	*	X_5	X_4	X_3	X_2	X_1	X_0		
1		*	*	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0		
1		*	*	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0		
1		*	*	*	*	*	*	P_{41}	P_{40}		

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	AB	1 *	0 *	1 X_5	0 X_4	1 X_3	0 X_2	1 X_1	1 X_0	Set Scroll Start	$X_5X_4X_3X_2X_1X_0$ specify the start block address (1 block = 4 lines) of area scrolling. Start block address = 000000b (POR)
0 1	20	0 *	0 *	1 *	0 *	0 X_3	0 X_2	0 X_1	0 X_0	Set Power Control Register	X_0=0: turns off the reference voltage generator (POR) X_0=1: turns on the reference voltage generator X_1=0: turns off the internal regulator and voltage follower (POR) X_1=1: turns on the internal regulator and voltage follower Select booster level X_3 X_2 Boost level 0 0 4X 0 1 5X 1 0 6X 1 1 7X
0 1 1	81	1 * *	0 * *	0 X_5 *	0 X_4 *	0 X_3 *	0 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Contrast Level & Internal Regulator Resistor Ratio	a) Select contrast level from 64 contrast steps Contrast increases as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 100000b (POR) b) The internal regulator gain (1+R2/R1) VOUT increases as $Y_2Y_1Y_0$ is increased from 000b to 111b. The factor, 1+R2/R1, is given by: $Y_2Y_1Y_0$ = 000: 6.49 (POR) $Y_2Y_1Y_0$ = 001: 7.03 $Y_2Y_1Y_0$ = 010: 7.80 $Y_2Y_1Y_0$ = 011: 8.91 $Y_2Y_1Y_0$ = 100: 9.37 $Y_2Y_1Y_0$ = 101: 10.53 $Y_2Y_1Y_0$ = 110: 11.13 $Y_2Y_1Y_0$ = 111: 12.02
0	D6 – D7	1	1	0	1	0	1	1	X_0	Increment / Decrement of the contrast set	X_0=0: The contrast set of voltage regulator is incremented by 1 X_0=1: The contrast set of voltage regulator is decremented by 1
0	A6 - A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
0 1 1	A8	1 X_7 Y_7	0 X_6 Y_6	1 X_5 Y_5	0 X_4 Y_4	1 X_3 Y_3	0 X_2 Y_2	0 X_1 Y_1	0 X_0 Y_0	Enter partial Display	$X_7X_6X_5X_4X_3X_2X_1X_0$: Start COM Address = 0000000b (POR) $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$: End COM Address = 0000000b (POR)
0	A9	1	0	1	0	1	0	0	1	Exit partial Display	Exit the “partial display mode” by executing the command 10101001b (POR)
0	AE - AF	1	0	1	0	1	1	1	X_0	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
0	94 - 95	1	0	0	1	0	1	0	X_0	Enter/Exit sleep mode	X_0=0: exit the sleep mode. X_0=1: enter sleep mode. (POR)
0	D1 - D3	1	1	0	1	0	0	X_1	X_0	Enable/disable internal oscillator	X_1 X_0 Internal oscillator status 0 1 ON 1 0 OFF (POR)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	82	1 *	0 *	0 *	0 *	0 *	0 *	1 X_1	0 X_0	Set Temperature compensation coefficient	Average temperature gradients X_1 X_0 Average Temperature Gradient [%/oC] 0 0 -0.13 0 1 -0.15 1 0 -0.20(POR) 1 1 -0.25
0 1	44	0 X_7	1 X_6	0 X_5	0 X_4	0 X_3	1 X_2	0 X_1	0 X_0	Set first display COM	$X_7X_6X_5X_4X_3X_2X_1X_0$ (0 to 131) specify one of ROW0-ROW131 to which the first display line (COM0) is mapped to
0 1 1 1 1	F4 05 58 03	1 0 0 0 0	1 0 0 1 0	1 0 0 0 0	1 0 X_4 1 0	0 0 0 1 0	1 1 0 0 0	0 0 0 0 1	0 1 0 0 1	Enable / Disable Vout discharging path	X_4 = 1: enable Vout discharging path X_4 = 0: disable Vout discharging path (POR) The Vout discharging path can be enabled when display changing from high mux (eg. 132 mux) to low mux (eg. 32 mux) in which Vout need to drop to relative low voltage in a short time.
0	25	0	0	1	0	0	1	0	1	NOP	Command result in No Operation. The command should be issued after the execution of the Status Read command
0 1	5C	0 Y_{71}	1 Y_{61}	0 Y_{51}	1 Y_{41}	1 Y_{31}	1 Y_{21}	0 Y_{11}	0 Y_{01}	Write display data	Enter the “write display data mode ” by executing the command 01011100b. The following byte is used to specify the data byte to be written to the GDDRAM directly. The D/C bit should be stated at logic “1” during the display data is written to the GDDRAM.

Remark: “” denote DON’T CARE* bit

Table 7 - Graphic command table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	83	1	0	0	0	0	0	1	1	Draw Line	Enter the "Draw line mode" by executing the command 10000011. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The remaining two bytes are used to specify the color. 16-bits color will be used for 18/16-bit pixel mode, 12 bit color will be used for 12/8-bit pixel mode.
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
		For 16-bit color									
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
		For 12-bit color									
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		*Remark:* *A, C ≤ 131, A < C; B, D ≤ 131, B < D*
0	92	1	0	0	1	0	0	1	0	Fill Enable/Disable	Enter the "Fill Enable/Disable mode" by executing the command 10010010. A_0=0: Filled color option is disabled (POR) A_0=1: Filled color option is enabled A_1=0: disable mix of ram content and graphic object (POR) A_1=1: enable mix of ram content and graphic object A_3A_2=00: no gradient fill (POR) A_3A_2=01: enable x-direction gradient fill A_3A_2=10: enable y-direction gradient fill A_3A_2=11: reserved A_5A_4=00: gradient color sources defined by two corner's colors in command 84 H(POR) A_5A_4=01: reserved A_5A_4=10: reserved A_5A_4=11: reserved A_6=0: dim to white (POR) A_6=1: dim to black
1		*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	84	1	0	0	0	0	1	0	0	Draw rectangle	Enter the "Draw rectangle mode" by executing the command 10000100. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The next two bytes are used to specify the border color. The last two bytes are used to specify the fill color. (depends on fill option of command 0x92). If gradient fill is enabled in command 0x92, the data byte which specific the border color is also used to specify the x,y coordinate of gradient start, and it should be within the rectangle.
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
		For 16-bit color									
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
		For 12-bit color									
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		*Remark:* *A, C ≤ 131, A < C; B, D ≤ 131, B < D*

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	86	1	0	0	0	0	1	1	0	Draw circle	Enter the "Draw circle mode" by executing the command 10000110. The first three bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7) are used to specify the centre's X coordinate, Y coordinate, circle's radius respectively. The next two bytes are used to specify the border color. The last two bytes are used to specify the fill color (depends on fill option of command 0x92).
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
		For 16-bit color									
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
1		R_4	R_3	R_2	R_1	R_0	G_5	G_4	G_3		
1		G_2	G_1	G_0	B_4	B_3	B_2	B_1	B_0		
		For 12-bit color									
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		
1		R_3	R_2	R_1	R_0	G_3	G_2	G_1	G_0		
1		*	*	*	*	B_3	B_2	B_1	B_0		*Remark:* *0 ≤ A7~A0 ≤ 255; 0 ≤ B7~B0 ≤ 255; 1 ≤ C7~C0 ≤ 255*
0	8A	1	0	0	0	1	0	1	0	Copy	Enter the "Copy mode" by executing the command. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The remaining two bytes (E_0 to E_7, F_0 to F_7) are used to specify the new location of X coordinates and Y coordinates.
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		*Remarks:* *A, C ≤ 131, A < C; B, D ≤ 131, B < D*
0	8C	1	0	0	0	1	1	0	0	Dim Window	Enter the "Dim Window mode" by executing the command 10001100. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The selected window area will be dimmed by 75% white or black according to data bit A6 of command 0x92
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		*Remarks:* *A, C ≤ 131, A < C; B, D ≤ 131, B < D*
0	8E	1	0	0	0	1	1	1	0	Clear Window	Enter the "Clear Window mode" by executing the command 10001110. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. All pixels contrast will be set to 0.
1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		*Remarks:* *A, C ≤ 131, A < C; B, D ≤ 131, B < D*

Remark: *"*" denote DON'T CARE* bit
After executed the graphic command, waiting time is required for update GDDRAM content.
(When V_{DD}=2.4~3.0V, waiting time = 340ns/pixel; When V_{DD}=3.0~3.6V, waiting time = 270ns/pixel)

Table 8 - Extended command table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	FB	1 *	1 *	1 *	1 *	1 0	0 0	1 B_1	1 B_0	Set biasing ratio	Allow user to set bias from 1/ 7 to 1/10 B_1B_0 Bias ratio 0 0 1/7 bias 0 1 1/8 bias 1 0 1/9 bias (POR) 1 1 1/10 bias
0 1 1	F2	1 0 0	1 0 N_6	1 0 N_5	1 0 N_4	0 F_3 N_3	0 F_2 N_2	1 F_1 N_1	0 F_0 N_0	Set Frame frequency and N-line Inversion	This command uses to change the frame frequency; set the N-line inversion and N-line inversion mode $F_3F_2F_1F_0$ 0 1 1 1 : 79.3 Hz 0 1 1 0 : 75.8 Hz 0 1 0 1 : 73.5 Hz (POR) 0 1 0 0 : 71.3 Hz 0 0 1 1 : 69.8 Hz The second byte data $N_5N_4N_3N_2N_1N_0$ sets the n-line inversion register from 2 to 64 lines to reduce display crosstalk. Register values from 000001b to 111111b are mapped to 2 lines to 64 lines respectively. Value 00000b disables the N-line inversion. 010000 is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux should NOT be a multiple of the lines of inversion (n). N_6 0 – reset n-line counter per frame (POR) 1 – will not reset n-line counter per frame Note: The frame frequency is measured at 7-line inversion condition and is calculated as 1 / ((Period of 7-line) * 132 / 7)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A2 - A3	1	0	1	0	0	0	1	X0	Reserved	
0 1 1 1	F7 28 05	1 0 X_7 0	1 0 0 0	1 1 0 0	1 0 0 0	0 1 1 0	1 0 1 1	1 0 1 0	1 0 X_0 1	Select PWM/FRC	X_7 0 0 0 1 1 1 X_0 0 0 0 0 1 1 1 0 : 5 bits PWM + 1 bit FRC (POR) 0 0 0 0 1 1 1 1 : 6 bits FRC 1 0 0 0 1 1 1 0 : 4 bits PWM + 2 bits FRC 1 0 0 0 1 1 1 1 : Reserved
0 1 1 1	F1 0 0	1 1 0 0	1 1 0 0	1 X_1 0 0	1 X_0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	Set COM sequence	X_1 X_0 COM0 – 65 COM66 - 131 0 0 : Normal Sequence Normal Sequence (POR) 0 1 : COM0 - COM31 COM32 - COM63, COM64 - COM97 COM98 - COM131 1 0 : COM1 - COM131 (odd) COM0 - COM130 (even) 1 1 : COM0 - COM130 (even) COM1 - COM131 (odd)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	F6	1	1	1	1	0	1	1	0	OTP setting	This command set the offset value of contrast
1		0	0	0	1	X_3	X_2	X_1	X_0		$X_3X_2X_1X_0Y_5$
1		0	0	Y_5	0	1	0	1	0		00000 : original contrast 00001 : original contrast + 1 step 00010 : original contrast + 2 steps 00011 : original contrast + 3 steps 00100 : original contrast + 4 steps 00101 : original contrast + 5 steps 00110 : original contrast + 6 steps 00111 : original contrast + 7 steps 01000 : original contrast + 8 steps 01001 : original contrast + 9 steps 01010 : original contrast + 10 steps 01011 : original contrast + 11 steps 01100 : original contrast + 12 steps 01101 : original contrast + 13 steps 01110 : original contrast + 14 steps 01111 : original contrast + 15 steps 10000 : original contrast - 16 steps 10001 : original contrast - 15 steps 10010 : original contrast - 14 steps 10011 : original contrast - 13 steps 10100 : original contrast - 12 steps 10101 : original contrast - 11 steps 10110 : original contrast - 10 steps 10111 : original contrast - 9 steps 11000 : original contrast - 8 steps 11001 : original contrast - 7 steps 11010 : original contrast - 6 steps 11011 : original contrast - 5 steps 11100 : original contrast - 4 steps 11101 : original contrast - 3 steps 11110 : original contrast -2 steps 11111 : original contrast - 1 step
0	F8	1	1	1	1	1	0	0	0	OTP programming	This command starts to program LCD driver with OTP offset value. Each bit can be programmed to 1 once. Detail of OTP programming procedure on page 48

Table 9 - Read Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	5D	0 D7	1 D6	0 D5	1 D4	1 D3	1 D2	0 D1	1 D0	Status Register Read	D7D6 = 00: Center Screen Scroll Mode D7D6 = 01: Top Screen Scroll Mode D7D6 = 10: Bottom Screen Scroll Mode D7D6 = 11: Whole Screen Scroll Mode D4 = 0: Scan Direction is column direction D4= 1: Scan Direction is page direction D3 = 0: Display is OFF D3 = 1: Display is ON D2 = 0: Sleep Mode is disabled D2 = 1: Sleep Mode is enabled D1 = 0: Display is Inverse D1 = 1: Display is Normal D0 = 0: Partial display is disabled D0 = 1: Partial display is enabled
0 1	5D	0 Y_{71}	1 Y_{61}	0 Y_{51}	1 Y_{41}	1 Y_{31}	1 Y_{21}	0 Y_{11}	1 Y_{01}	Read display data	Enter the “read display data mode ” by executing the command 01011101b. The next byte is a dummy data. The GDDRAM data will be read form the second byte. The GDDRAM column address pointer will be increased by one automatically after each 2-bytes data read. (65K color mode).

Note: Command patterns other than that given in Command Table are prohibited. Otherwise, unexpected result will occur.

Remark: “” denote DON’T CARE* bit

8.1 Data Read / Write

To read data from the GDDRAM, 5DH command should be executed then input High to R/$\overline{W}$ ($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode. Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read in 8-levels gray scale mode OR after each 3-bytes data read in 16-levels gray scale mode. Also, a dummy read is required before the first data is read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/$\overline{W}$ ($\overline{WR}$) pin and High to D/$\overline{C}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write in 8-levels gray scale mode OR each 3-bytes data write in 16-levels scale mode. The address will be reset to 0 in next data read/write operation is executed when it is 131.

9 COMMAND DESCRIPTIONS

9.1 Set Column Address (15 Hex)

This command specifies the 8-bit column address of the display data RAM. The start and the end column address are specified by this command. The driver supports up to 132 columns. As the addresses are incremented from the start column to the end column in the column direction scan, the page address is incremented by 1. The column address is then returned to the start column. The column address will be increased by each data access after it is preset by the MCU. Start column < End column must be maintained.

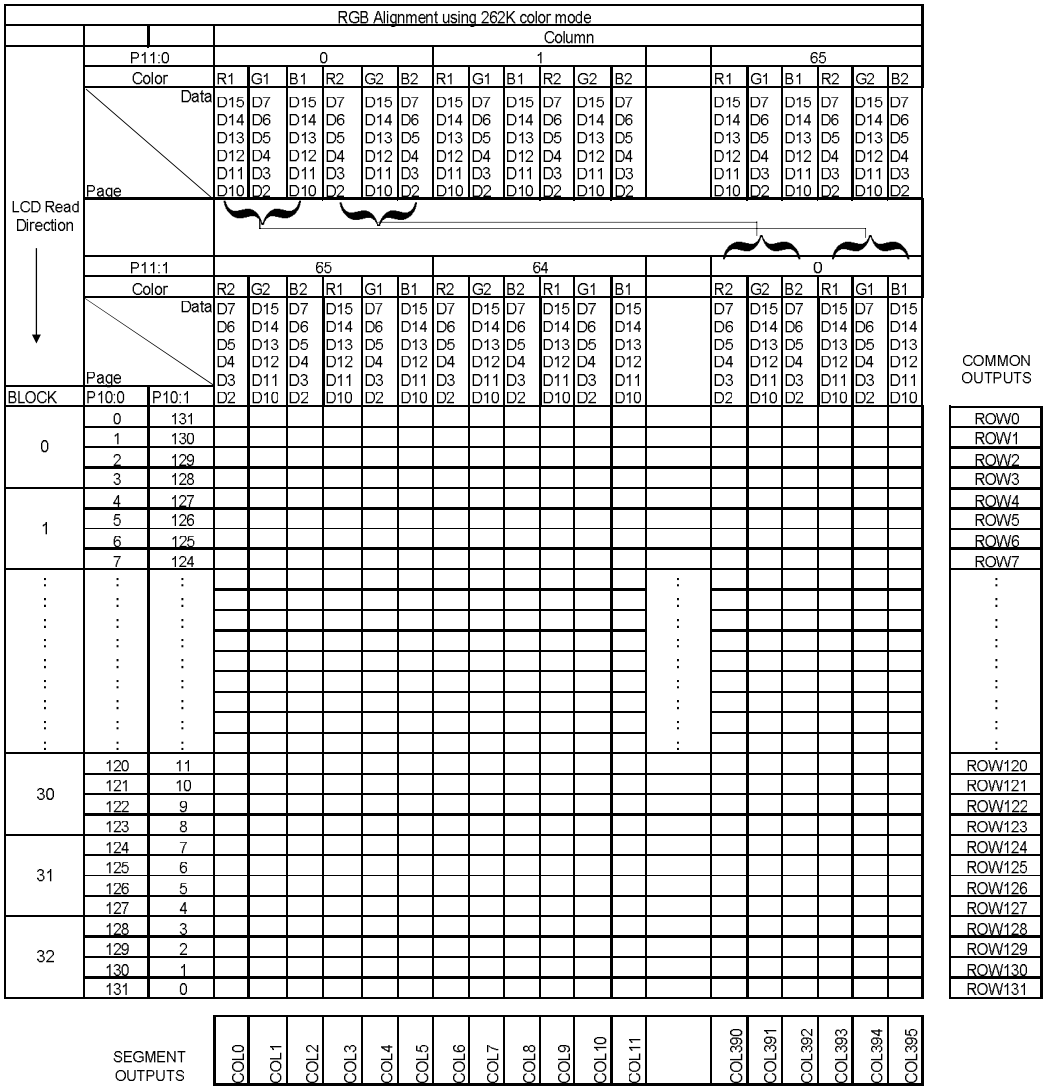


Table 10 - RAM arrangements of 18-bit/pixel, direct write mode.

9.2 Set Page Address (75 Hex)

This command enters the page address from 0 to 131 to the RAM page register for read/write operations. The driver supports up to 132 lines. All in all, there are 132 pages. As the addresses are incremented from the start page to the end page in the page direction scan, the column address is incremented by 1. The page address is then returned to the start page. Start page < End page must be maintained.

9.3 Set COM Output Scan Direction (BB Hex)

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. Please refer to the Table 6 on Page 26 for detail mapping. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

9.4 Set Data Output Scan Direction (BC Hex)

This command sets the DDRAM such that the MPU operates the display data in the internal RAM.

A. Normal or Inverse page/column/scan directions
The Data Scan direction can be set to either normal or inverse display page and column address scan direction. The column and the page direction are illustrated in the following figure and
Figure 8 on page 39 for the example of normal or inverse page/column/ scan directions.

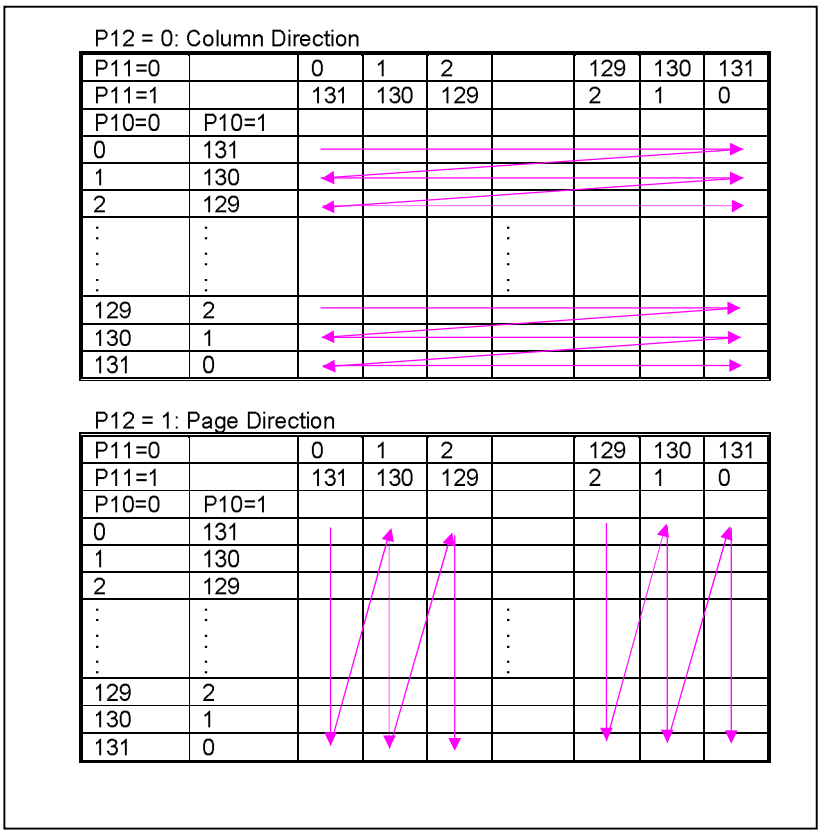


Figure 7 - Column and page scan direction

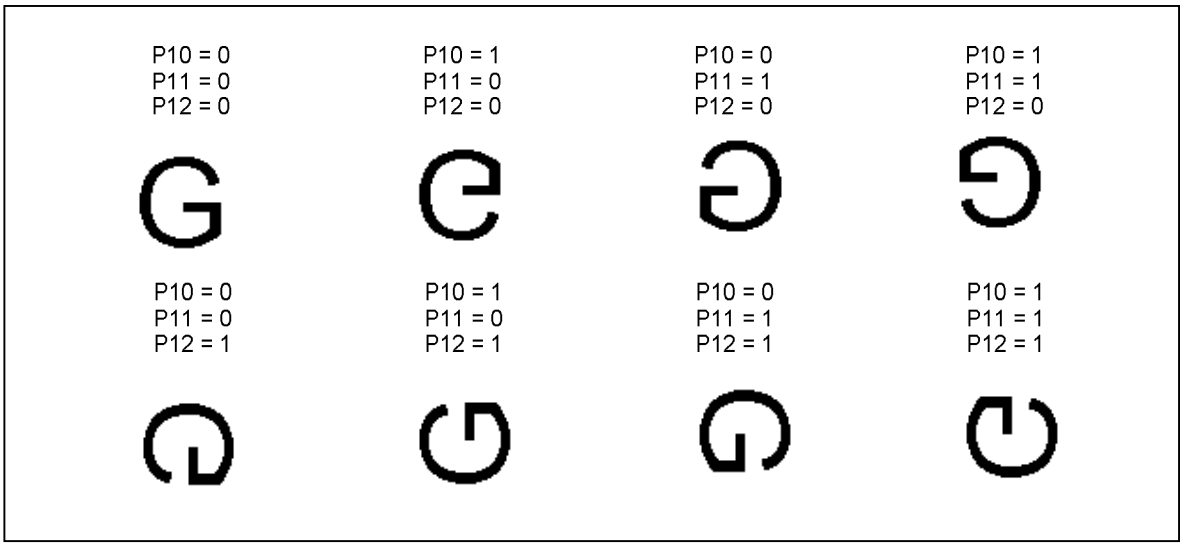


Figure 8 - Example of Normal or Inverse page/column/ scan directions

The parameters following the command set data output scan direction specifies the RGB arrangement and the selection of various gray-scale modes. Please find the information of the RGB arrangement and the gray scale mode in the following section.

B. RGB arrangement mode
The RGB arrangement mode can be selected according to the following table. Three selection bits will give eight combinations of the RGB arrangements. Each combination set will specify the Red, Green and Blue segment output arrangement in odd and even page.

P_{22}, P_{21}, P_{20}	LINE	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	…	COL395
000 (POR)	Even page Odd page	R R	G G	B B	R R	G G	B B	R R	G G	…	B B
001	1 2	B B	G G	R R	B B	G G	R R	B B	G G	…	R R
010	1 2	R R	G G	B B	B B	G G	R R	R R	G G	…	R R
011	1 2	B B	G G	R R	R R	G G	B B	B B	G G	…	B B
100	1 2	R B	G G	B R	R B	G G	B R	R B	G G	…	B R
101	1 2	B R	G G	R B	B R	G G	R B	B R	G G	…	R B
110	1 2	R B	G G	B R	B R	G G	R B	R B	G G	…	R B
111	1 2	B R	G G	R B	R B	G G	B R	B R	G G	…	B R

Table 11 - RGB Arrangement modes

C. Gray scale mode
Gray scale selection and corresponding data bus arrangement for different bus interface mode are illustrated in the following table.

P31, P30	Gray Scale selection	Bus interface mode (select by PS2-PS0, ref to Table 3)	P34, P33	Data bus arrangement (D15……D0) for 16 bit bus mode, (D7……D0) for 8 bit bus mode ("*" denote don't care bit)	Note
00	16-bit / pixel	16 bit	**	RRRRRGGGGGGBBBBB	1 word / 1 pixel
		8 bit		RRRRRGGG (byte 1) GGGBBBBB (byte 2)	2 byte/ 1 pixel
01	8-bit / pixel	8 bit	**	RRRGGGBB	1 byte / 1 pixel
10	12-bit / pixel	16 bit	**	RRRRGGGGBBBB****	1 word / 1 pixel
		8 bit		RRRRGGGG (byte 1) BBBBRRRR (byte 2) GGGGBBBB (byte 3)	3 byte / 2 pixel
11	18-bit / pixel	16 bit	00	RRRRRR**GGGGGG** (word 1) BBBBBB**RRRRRR** (word 2) GGGGGG**BBBBBB** (word 3)	3 word / 2 pixel
			01	RRRRRR**GGGGGG** (word 1) ********BBBBBB** (word 2)	2 word / 1 pixel
			11	RRRRRR**GGGGGG** (word 1) BBBBBB********** (word 2)	2 word / 1 pixel
		8 bit	**	RRRRRR** (byte 1) GGGGGG** (byte 2) BBBBBB** (byte 3)	3 byte / 1 pixel

Table 12 - Data bus arrangement for different pixel and bus mode

9.5 Set Color Look Up Table (CE Hex)

This command is used to set the color look up table (LUT) for different pixel mode. The LUT has 32 6-bit entries, the number of entry to write depends on different pixel mode, the 6 LSB of each of the data byte following this command correspond to one entry of the LUT.

Pixel mode	No. of entry	Note
18 or 16 bit/pixel	32	32 data byte (6 LSB of each) define the LUT
12 bit/pixel	16	16 data byte (6 LSB of each) define the LUT
8 bit/pixel	10	10 data byte (6 LSB of each) define the LUT with 1st 8 byte define all 8 colors of Red and Green, while Blue will use 1st and 8th byte for data 00, 11 correspondingly, and will use 9th and 10th byte for data 01 and 10 correspondingly.

9.6 Set Display Control (CA Hex)

This command is used to select the duty ratio of the IC. All available driving duty can be selected using this command. The driving duty can be changed from 1/32 to 1/132.

9.7 Set Area Scroll (AA Hex)

This command specifies the portion of screen for scrolling. The command sets the starting block address, finishing block address, number of specific blocks and the area scroll mode of the area scrolling. Please be noted that the starting block address should be smaller than the finishing block address.
The block address increment direction is started at 0th block such that the GDDRAM address corresponds to the top of the fixed area. Similarly, the block address decrement direction is started at the 41st block such that the GDDRAM address corresponds to the bottom fixed area. The remaining block address excluding the top and the bottom fixed areas are assigned to the scroll plus the background areas.
The set area scroll function is divided into four parts.

Part I -Specify the top block address of the scroll + the background areas. Specify the 0th block for the top screen scroll or the whole screen scroll. The scroll start block address is also set at this top block address until the scroll start set command is executed.

Part II – Specify the bottom address of the scroll + background areas. Specify the 32nd block for the bottom or the whole screen scroll.

Part III – Specify number of scrolled blocks = number of (Top fixed area + scroll area) blocks –1. When the bottom scroll or whole screen scroll is chosen, the resulted value is identical to the value stated in part II.

Part IV

Specify the area scroll type. Altogether there are four types of area scroll. Please refer to Table 13 for detail.

P41	P40	Types of Area Scroll
0	0	Center Screen Scroll
0	1	Top Screen Scroll
1	0	Bottom Screen Scroll
1	1	Whole Screen Scroll

Table 13 - Area scrolling selection modes

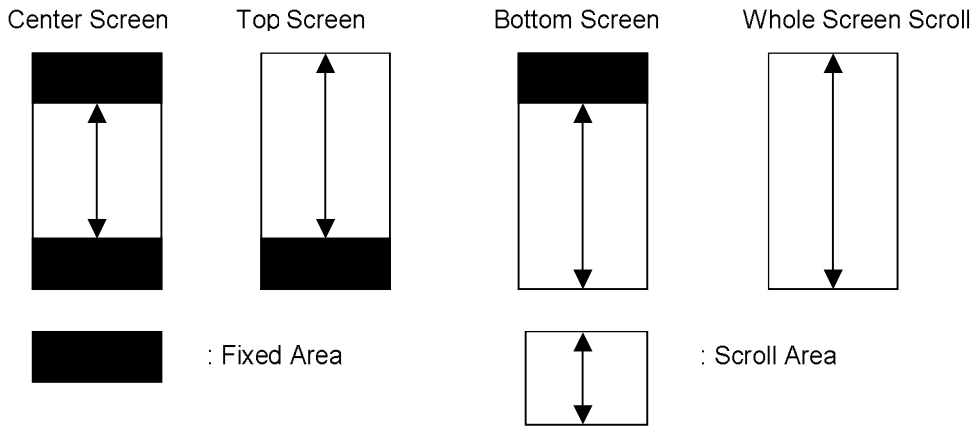


Figure 9 - Area scrolling selection modes

The area scroll function is executed by prompt in the set area scroll command following by changing the start block address by the set scroll start command. The above

Figure 9 illustrates the operation model of the scrolling function.

Example: In the Center screen scroll of 1/96 duty (display range: 96 lines = 24 blocks)

Description	Command	Data
- Set Area Scroll	AA Hex	
- 8 lines (block 0 and block 1) is specified for the top fixed area Top block address = Number of lines in top fixed area / 4 = 8 / 4 = 2		02 Hex
- 8 lines (block 31 & block 32) are specified for the bottom fixed area Bottom block address = 32 – (number of lines in bottom fixed area / 4) = 32 – (8 / 4) = 32 – 2 = 30		1E Hex
- 80 lines (block 2 to block 21) are specified the scroll area Number of specified block = Top block address + (number of lines in scroll area/4) – 1 = 2 + (80 / 4) –1 = 2 + 20 – 1 = 21		15 Hex
- 36 lines (block 22 to block 30) are specified the background areas		
- Set area scroll mode – Center screen mode		00 Hex
- Set Scroll start (Scroll range form 02H ~ 1EH)	ABH	
		02 Hex

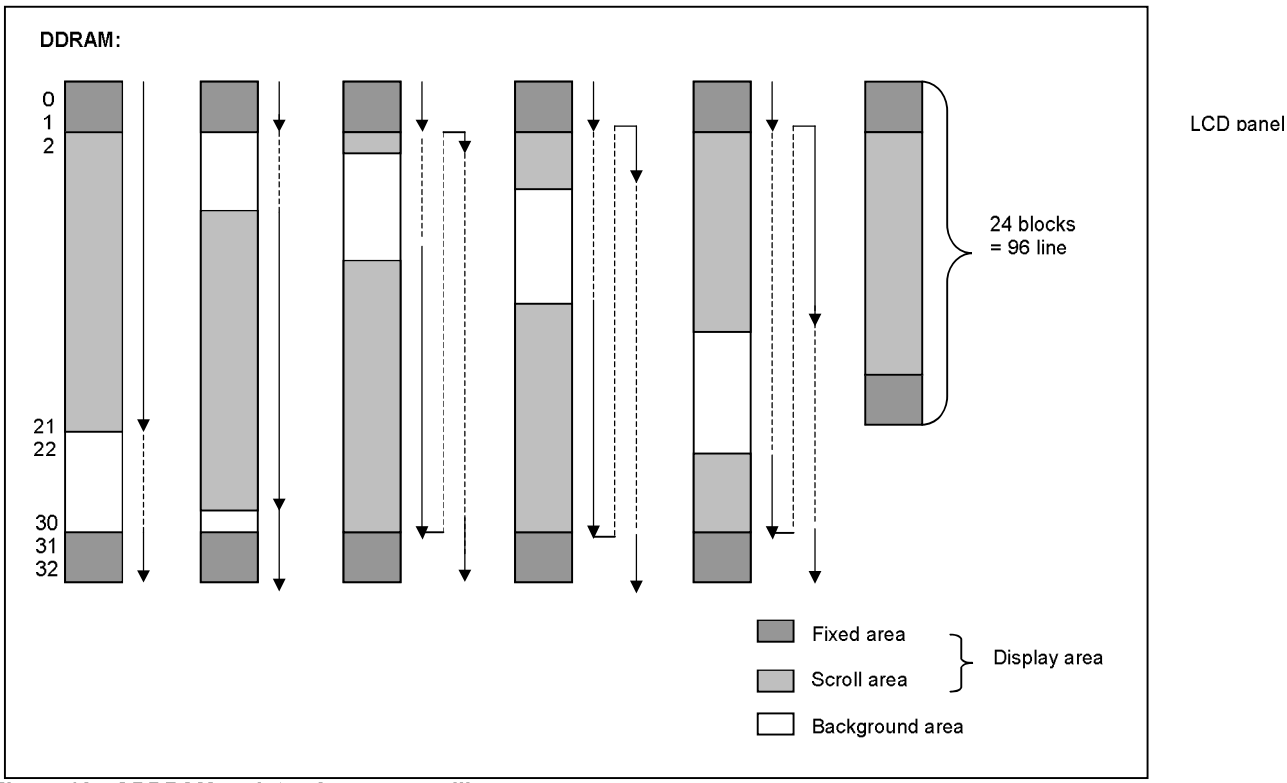
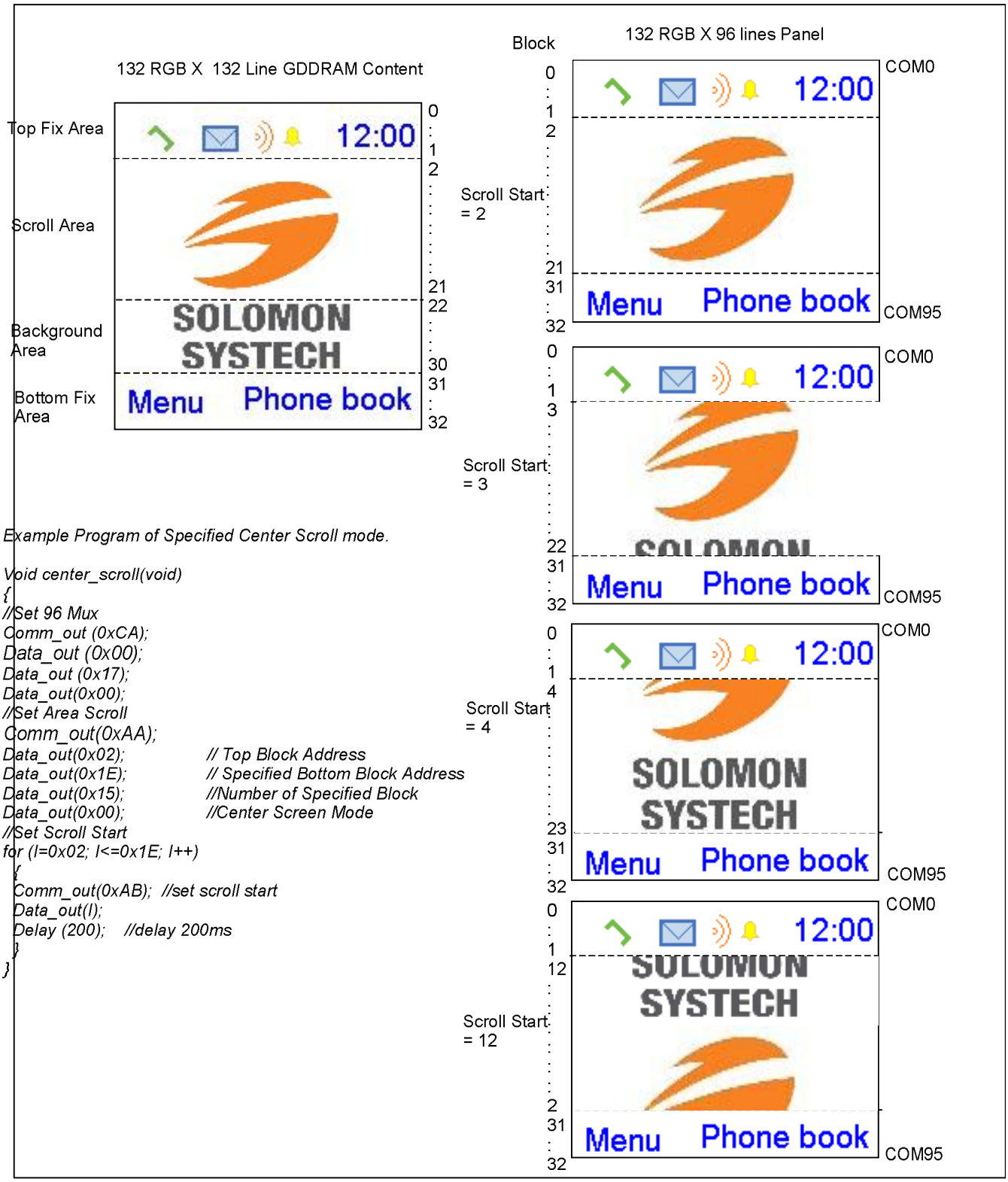


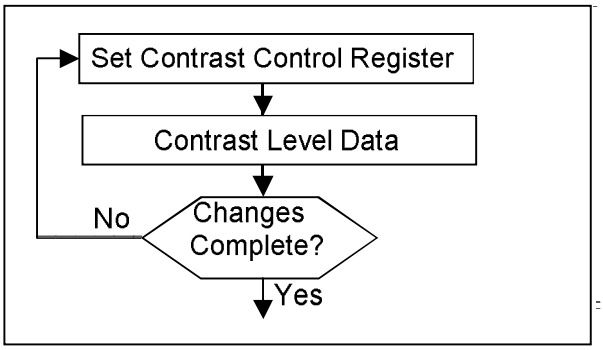
Figure 10 - GDDRAM updates for area scrolling



Example Program of Specified Center Scroll mode.

```
Void center_scroll(void)
{
//Set 96 Mux
Comm_out (0xCA);
Data_out (0x00);
Data_out (0x17);
Data_out(0x00);
//Set Area Scroll
Comm_out(0xAA);
Data_out(0x02);          // Top Block Address
Data_out(0x1E);          // Specified Bottom Block Address
Data_out(0x15);          //Number of Specified Block
Data_out(0x00);          //Center Screen Mode
//Set Scroll Start
for (I=0x02; I<=0x1E; I++)
  {
  Comm_out(0xAB);  //set scroll start
  Data_out(I);
  Delay (200);    //delay 200ms
  }
}
```

Figure 11 - Example of center scroll mode



$$V_{OUT} = (1 + R_2/R_1) * V_{CON}$$

$$V_{CON} = (1 + \alpha / 260) * V_{REF}$$, where V_{REF} = 1.105V at TC0,

Please refer to **Table 15-DC Characteristic** for V_{REF} at other TC values.

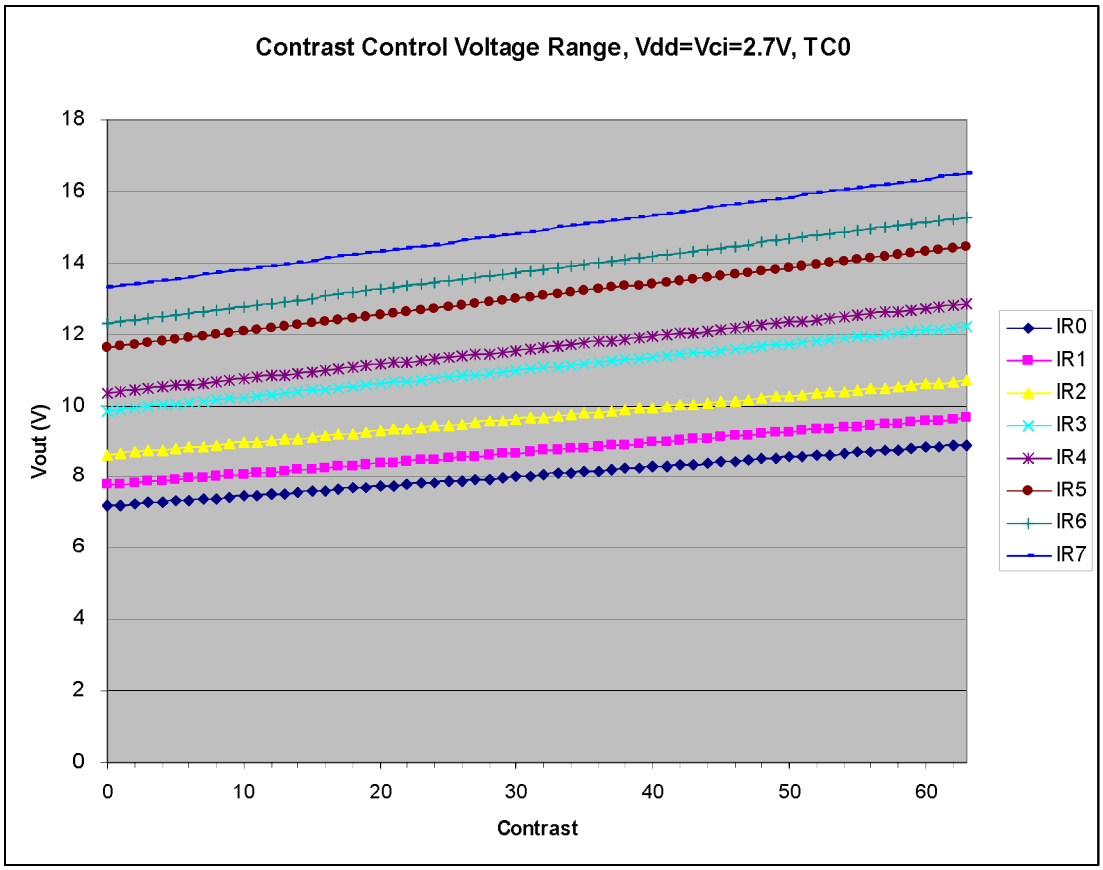


Figure 13 - Contrast Control Voltage Range Curve (Vdd=Vci=2.7V, TC0)

9.11 Set Increment/Decrement of the contrast (D6/D7 Hex)

This command can increase the contrast step by +1 (D6 Hex) and decrease the contrast step by –1 (D7 Hex). It is the most convenient way to change the contrast of the display by programming.

9.12 Set Normal/Inverse Display (A6/A7 Hex)

This command turns the display to be either normal (A6 Hex) or inverse (A7). In normal display mode, a RAM data of 1 indicates an illumination on the corresponding pixel in the normal white panel. In inverse display mode, a RAM data of 0 will turn on the pixel. It should be noted that the icon line is not affected. The icon line is not inversed by this command.

Example:
For a normal white display panel (Set Normal Display: A6Hex):

RAM Content			Color
R	G	B	
0	0	0	White
F	F	F	Black
0	F	F	Red
F	0	F	Green
F	F	0	Blue

For a normal black display panel (Set Normal Display: A7Hex):

RAM Content			Color
R	G	B	
0	0	0	White
F	F	F	Black
0	F	F	Red
F	0	F	Green
F	F	0	Blue

9.13 Enter Partial Display (A8 Hex)

This command and the following parameters specify the display area of the partial display mode. The following figure shows the display and non-display area when the partial display mode is executed.

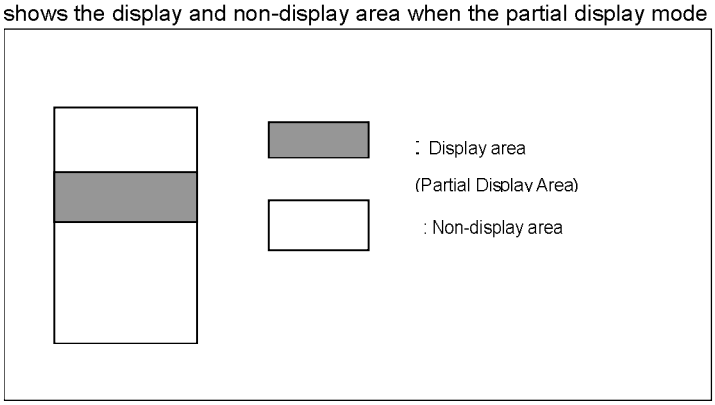


Figure 14 - Partial display mode

9.14 Exit Partial Display (A9 Hex)

This command exits the partial display mode.

9.15 Set Display On/Off (AF/AE Hex)

This command is used to turn the display on (AF Hex) or off (AE Hex). When display off is issued with entire display is on, power save mode will be entered.

9.16 Enter/Exit sleep mode (95/94 Hex)

This command enter (95 Hex) or exit (94 Hex) the sleep mode.

9.17 Enable/Disable the internal oscillator (D1/D2 Hex)

This command enables (D1 Hex) or disables (D2 Hex) the internal oscillator. The internal oscillator is turned off after reset.

9.18 Set Temperature compensation coefficient (82 Hex)

This command sets the average temperature gradients. Four sets of average temperature gradients can be selected. Please refer to the command table for detail description of the average temperature gradients. The default value of the temperature gradient is –0.20 %/^{0}C

9.19 Set First Display COM (44 Hex)

This command map the first display COM data to one of ROW0 – ROW131.

9.20 Enable/Disable Vout discharging path (F4 Hex)

This command enable/disable Vout discharging path. The Vout discharging path can be enabled when display is changing from high mux (eg. 132 mux) to low mux (eg. 32 mux) in which Vout need to drop to a low voltage in a short time.

9.21 NOP (25 Hex)

A command causing the chip takes No Operation.

9.22 Write display data mode (5C Hex)

This command is used to execute the write display data mode. The display data byte is directly written to the GDDRAM. Please be noted that the D/$\overline{C}$ signal should be set to high during the display data is written to the GDDRAM.

9.23 Read display data mode (5D Hex)

This command is used to execute the read display data mode. The display data byte is directly read from the GDDRAM. Please be noted that the D/$\overline{C}$ signal should be set to high during the display data is red from to the GDDRAM.

9.24 Set biasing ratio (FB Hex)

This command selects a suitable bias ratio (1/7 to 1/10) required for driving the particular LCD panel in use.

9.25 Set Frame Frequency (F2 Hex)

This command specifies the frame frequency so as to minimize the flickering due to the ac main frequency. The frequency is set to 75 Hz after POR.

9.26 Set N-line inversion (F2 Hex)

Number of line inversion is set by this command for reducing crosstalk noise. 2 to 64-line inversion operations could be selected. At POR, this operation is set to 10000b (17 lines). It should be noted that the total number of mux (including the icon line) should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change. The n-line counter can be set such that it will be reset per display frame (POR).

9.27 Select PWM/FRC (F7 Hex)

This command set the Pulse Width Modulation, Frame Rate Control or mix of FWM & FRC.

9.28 OTP setting (F6 Hex)

OTP (One Time Programming) is a method to adjust V_{OUT}. In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules. Each OTP bit can be programmed to '1' one time.

OTP setting and programming should include two major steps. Find the OTP offset and OTP programming as following,

Step 1. Find OTP offset

(1) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Adjust the contrast value (C:0x81, D:0x00~0x3F, D: 0x00 ~ 0x07) until there is the best visual contrast
(5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x24
OTP offset value = 0x24 - 0x20 = +4
OTP setting command should be (C: 0xF6, D: 0x12, D: 0x0A)

Example 2:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x1B
OTP setting = 0x1B - 0x20 = -5
OTP setting command should be (C:0xF6, D: 0x1D, D: 0x2A)

Step 2. OTP programming

(6) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(7) Enable Oscillator (C: 0xD1) and Exit Sleep Mode (C: 0x94)
(8) Connect an external V_{OUT} (see diagram below)
(9) Send OTP setting commands that we find in step 1 (C: 0xF6, D: 0x10~0x1F, D: 0x0A~0x2A)
(10) Send OTP programming command (C: 0xF8)
(11) Wait at least 2 seconds
(12) Hardware Reset
(13) Verify the result by repeating step 1. (2) – (3)

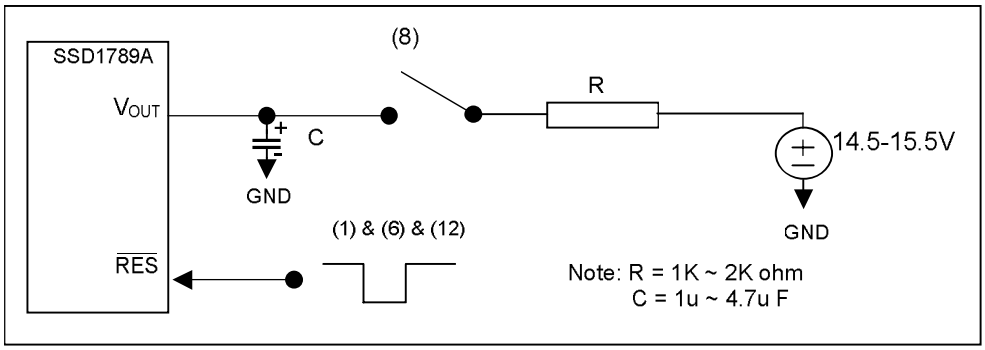


Figure 15 - OTP programming circuitry

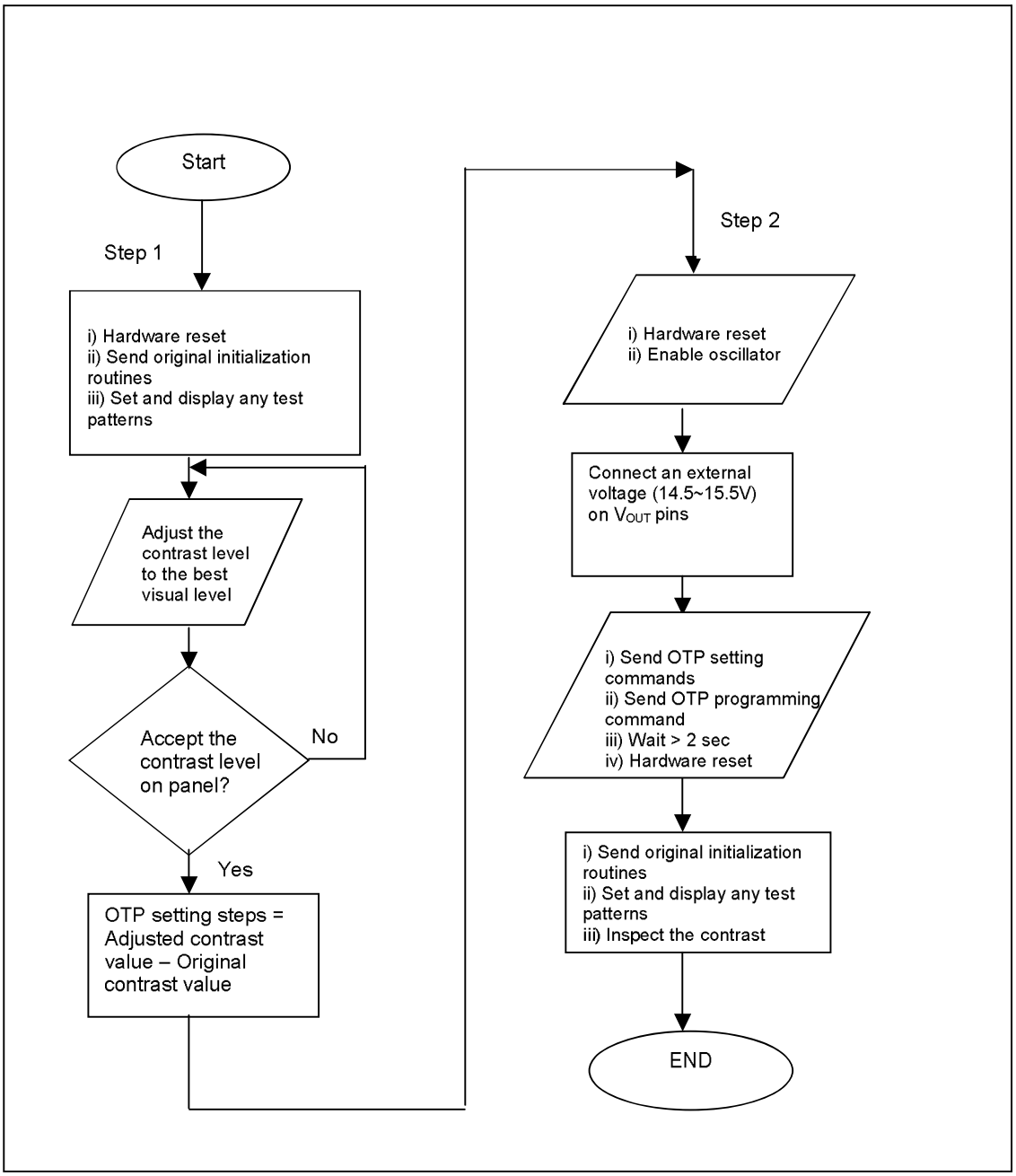


Figure 16 - Flow chart of OTP programming Procedure

OTP Example program

Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
2. COMMAND(0XD1); \\Enable oscillator;
   COMMAND(0X94); \\ exit sleep mode;
3. COMMAND(0X20); \\ turn on the reference voltage generator, internal regulator and voltage follower; Select booster level.
   DATA(0x0F);
4. COMMAND(0XFB) \\ Set Biasing ratio
   DATA(0X2) \\ 1/9
5. COMMAND(0X81) \\Set target gain and contrast.
   DATA(0X14) \\ contrast = 20
   DATA(0X05) \\ Internal Regulator Gain = 11.57
6. \\ Set target display contents
   COMMAND(0X15) \\ set column address
   DATA(0x00) \\ set start column address at 0
   DATA(0X83) \\ set end column address at 131
   COMMAND(0X75) \\ set page address
   DATA(0X00) \\ set start page address at 0
   DATA(0X83) \\ set end page address at 131
   COMMAND(0X5C) \\ write target content to GDDRAM
   DATA(…)
   COMMAND(0xAF) \\ display on
7. OTP offset calculation… target OTP offset value is +3

OTP programming:

8. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
9. COMMAND(0XD1) \\ Enable Oscillator
10. COMMAND(0x94) \\ Exit Sleep Mode
11. Connect a external V_{OUT} (14.5V~15.5V)
12. COMMAND(0XF6) \\ Set OTP offset value to +3 (0011)
    DATA(0X11) \\ 00011 $X_3X_2X_1X_0Y_5$, where $X_3X_2X_1X_0Y_5$ is the OTP offset value
    DATA(0x2A)
13. COMMAND(0XF8) \\ Send the OTP programming command.
14. Wait at least 2 seconds for programming wait time.

Verify the result:

15. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel.

9.29 Draw Line (83 Hex)

Given the starting point (X1, Y1) and the ending point (X2, Y2), a line will be drawn with the color specified.

The following example illustrates the line drawing procedure.

1. Enter the “draw line mode” by execute the command 83H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 01H
5. Set the finishing Y-coordinates, Y2. E.g., 01H
6. Set the color to RGB = (0,1,0) e.g., 07H followed by E0H

Result: A green line will be drawn between coordinates (0,0) and (1,1)

Remark: X1, X2 ≤131; X1 < X2

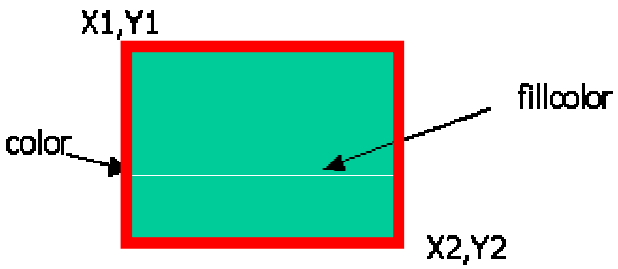
Y1, Y2 ≤131; Y1 < Y2

9.30 Fill Enable/Disable (92 Hex)

This command allows the fill color option to be enabled or disabled. This command is applicable to the Draw Rectangle feature. When the selection bit is “0”, the fill color option is disabled. When the selection bit is “1”, the fill color option is enabled.

9.31 Draw rectangle (84 Hex)

Given the starting point (X1, Y1) and the ending point (X2, Y2), specify the width and height of a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.



The following example illustrates the rectangle drawing procedure.

1. Enter the “draw rectangle mode” by execute the command 8AH
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 02H
5. Set the finishing Y-coordinates, Y2. E.g., 02H
6. Set the color to RGB = (1,0,0) e.g., F8H following by 00H
7. Set the filled color to RGB = (0,1,0) e.g., 07H following by E0H

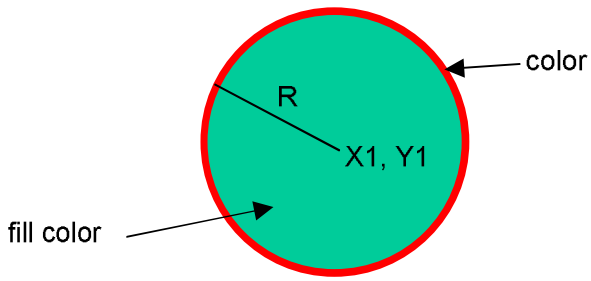
Result: A rectangle will be drawn at (0,0) to (2,2), filled green with red border

Remark: X1, X2 ≤131; X1 < X2

Y1, Y2 ≤131; Y1 < Y2

9.32 Draw Circle (86 Hex)

Given the center point (X1, Y1) and the radius R, a circle will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.



The following example illustrates the rectangle drawing procedure.

1. Enter the “draw circle mode” by execute the command 86H
2. Set the center X-coordinates, X1. E.g., 40H.
3. Set the center Y-coordinates, Y1. E.g., 40H.
4. Set the radius, R. E.g., 20H
5. Set the color to RGB = (1,0,0) e.g., F8H following by 00H
6. Set the filled color to RGB = (0,1,0) e.g., 07H following by E0H

Result: A circle will be drawn with center (64,64) and radius 32, filled green with red border

Remark: 0 ≤X1,Y1 ≤255

1 ≤R ≤255

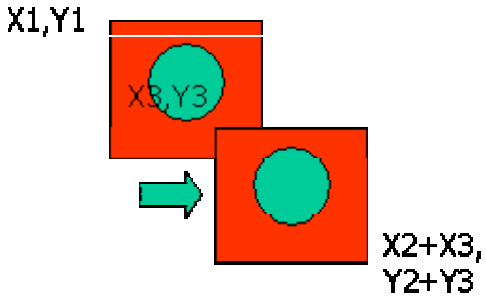
9.33 Copy (8A Hex)

Copy the rectangular region defined by the starting point (X1, Y1) and the ending point (X2, Y2) to location (X3, Y3). There are two possible results with the command copy executed depending on the setting of the start point coordinates and end point coordinates.

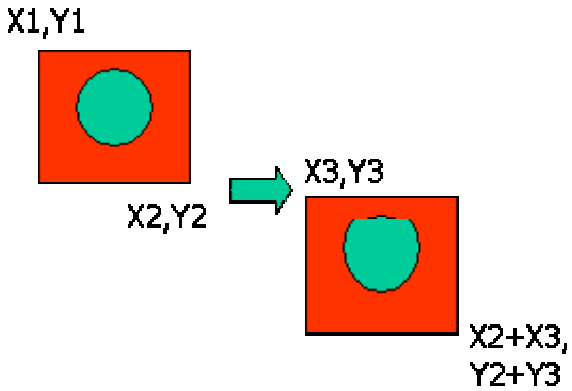
The following example illustrates the copy procedure.

Case 1 – The overlap region will superimpose.

1. Enter the "copy mode" by execute the command 84H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 02H
5. Set the finishing Y-coordinates, Y2. E.g., 02H
6. Set the New X-coordinates, X3. E.g., 01H
7. Set the New Y-coordinates, Y3. E.g., 01H



Case 2 – The original content remains unchanged



1. Enter the "copy mode" by execute the command 84H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 01H
5. Set the finishing Y-coordinates, Y2. E.g., 01H
6. Set the New X-coordinates, X3. E.g., 09H
7. Set the New Y-coordinates, Y3. E.g., 09H

Remark: X1, X2 ≤131; X1 < X2
Y1, Y2 ≤131; Y1 < Y2

9.34 Dim Window (8C Hex)

This command will dim the window area specify by starting point (X1, Y1) and the ending point (X2, Y2). After the execution of this command, the selected window area will be dimmed by 75% white. Additional execution of this command over the same window area will not change the data content.

Remark: X1, X2 ≤131; X1 < X2
Y1, Y2 ≤131; Y1 < Y2

9.35 Clear Window (8E Hex)

This command sets the window area specify by starting point (X1, Y1) and the ending point (X2, Y2) to clear the window display. The GDDRAM content of the window will be set to zero.

Remark: X1, X2 ≤131; X1 < X2
Y1, Y2 ≤131; Y1 < Y2

9.36 Status register read

The following parameters can be monitored by the status read register.

1. Various area scroll mode
2. Column scan direction
3. Page scan direction
4. Display ON/OFF
5. Sleep mode ON/OFF
6. Display Normal/Inverse
7. Partial display mode ON/OFF

10 MAXIMUM RATINGS

Table 14 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{OUT}		-0.3 to 18	V
V_{CI}	Input Voltage	VSS-0.3 to 4.0	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
Ron	Input Resistance	1000	ohm

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} and V_{OUT} be constrained to the range $V_{SS} < V_{DD} \leq V_{CI} < V_{OUT}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Table 15 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.6V, T_A = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	System power supply pins of the logic block Range	Recommend Operating Voltage Possible Operating Voltage	2.4	2.7	3.6	V
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.2	V_{DD}	V_{DD}	V
V_{CI}	Booster Reference Supply Voltage Range (3)	Recommend Operating Voltage Possible Operating Voltage	V_{DD}	V_{DD}	3.6	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 7X DC-DC , 16-bit 8080 parallel bus writing AAAA HTcyc =3MHz, Typ. Osc. Freq., Display On, no panel attached.	-	650	1150	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{OUT} = 16V, Voltage Generator On, 7X DC-DC Converter Enabled, R/W(WR) Halt, Typ. Osc. Freq., Display On, no panel attached.	-	500	1000	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, R/W(WR) halt.	-	2	5	µA
V_{OUT}	LCD Driving Voltage Generator Output (V_{OUT} Pin)	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	8	-	16	V
V_{REF}	Internal Reference Voltage (T=25 °C)	TC0 = -0.13%/°C TC1 = -0.15%/°C TC2 = -0.20%/°C (POR) TC3 = -0.25%/°C	1.072 1.080 1.101 1.117	1.105 1.113 1.135 1.152	1.138 1.146 1.169 1.187	V
V_{OH1}	Logic High Output Voltage	Iout=-100µA	0.9* V_{DD}	-	V_{DD}	V
V_{OL1}	Logic Low Output Voltage	Iout=100µA	0	-	0.1*V_{DD}	V
V_{IH1}	Logic High Input voltage		0.8* V_{DD}	-	V_{DD}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2* V_{DD}	V
I_{OH}	Logic High Output Current Source	V_{OUT} = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	V_{OUT} = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
ΔV_{OUT}	Variation of V_{OUT} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-2	0	2	%
R_O	SEG/COM output resistance		-	500	-	ohm
TC0	Average Temperature Gradient Flat Temperature Coefficient	Voltage Regulator Enabled	-0.10	-0.13	-0.14	%/°C
TC1	Temperature Coefficient 1*		-0.14	-0.15	-0.18	%/°C
TC2	Temperature Coefficient 2* (POR)		-0.18	-0.20	-0.23	%/°C
TC3	Temperature Coefficient 3*		-0.23	-0.25	-0.28	%/°C

*The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref} \text{ at } 50^{o}C - V_{ref} \text{ at } 0\ ^{o}C}{50\ ^{o}C - 0\ ^{o}C} \times \frac{1}{V_{ref} \text{ at } 25\ ^{o}C} \times 100\ \%$$

12 AC CHARACTERISTICS

Table 16 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.7V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{FRM}	POR Frame Frequency for: 132 MUX Mode	132 RGB x 132 Graphic Display Mode, Display ON, Internal Oscillator Enabled. POR frequency. 7-line inversion. The frame frequency is calculated as 1 / ((Period of 7-line) * 132 / 7)	71.5	73.5	75.5	Hz

Table 17 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	130	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	200	ns
t_{OH}	Output Hold time	20	-	60	ns
PW_{CSH}	Chip Select High Pulse Width (write cycle)	65	-	-	ns
PW_{CSL}	Chip Select Low Pulse Width (write cycle)	65	-	-	ns

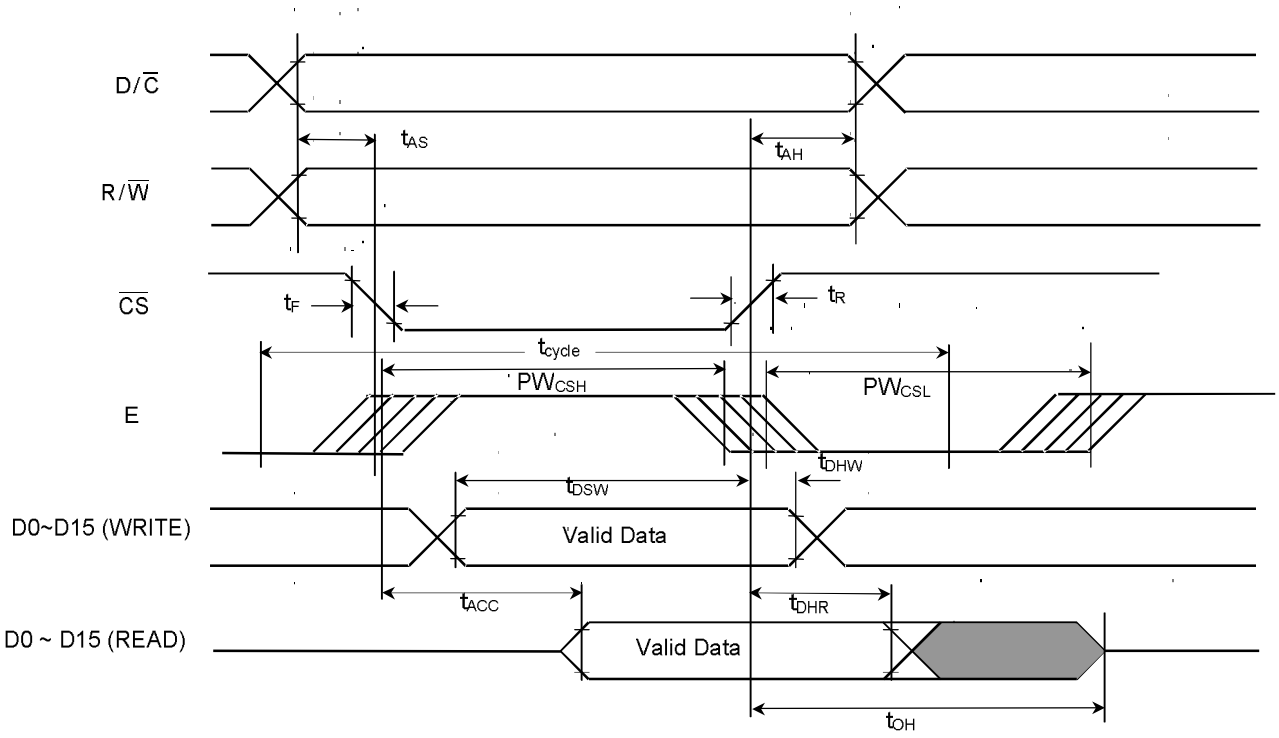
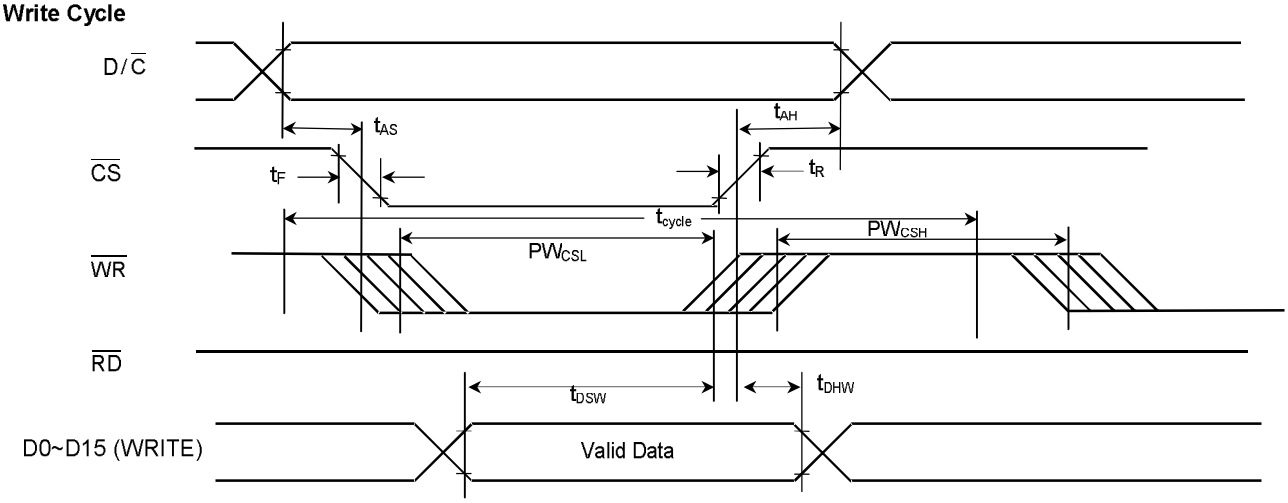


Figure 17 - 8-bit/16-bit Parallel 6800-series Interface Timing Characteristics

Table 18 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	130	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns
PW_{CSH}	Chip Select High Pulse Width (write cycle)	65	-	-	ns
PW_{CSL}	Chip Select Low Pulse Width (write cycle)	65	-	-	ns

Write Cycle



Read Cycle

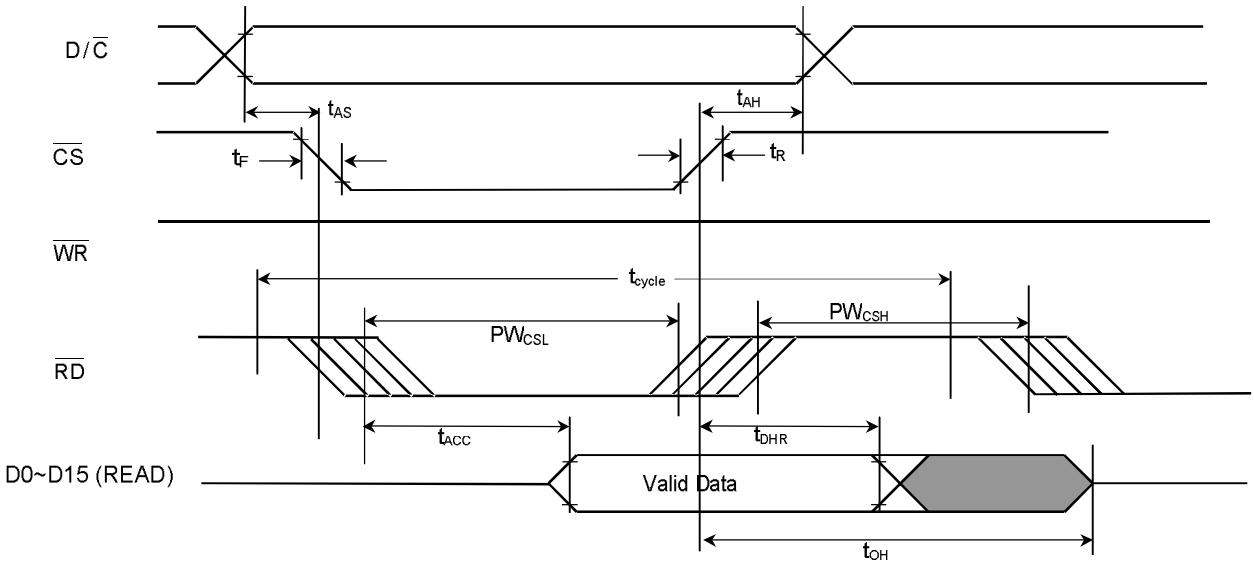


Figure 18 - 8-bit/16-bit Parallel 8080-series Interface Timing Characteristics

Table 19 – Parallel Timing Characteristics (TA = -40 to 85°C, V_{DD} = 2.4V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	250	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns
PW_{CSH}	Chip Select High Pulse Width (write cycle)	125	-	-	ns
PW_{CSL}	Chip Select Low Pulse Width (write cycle)	125	-	-	ns

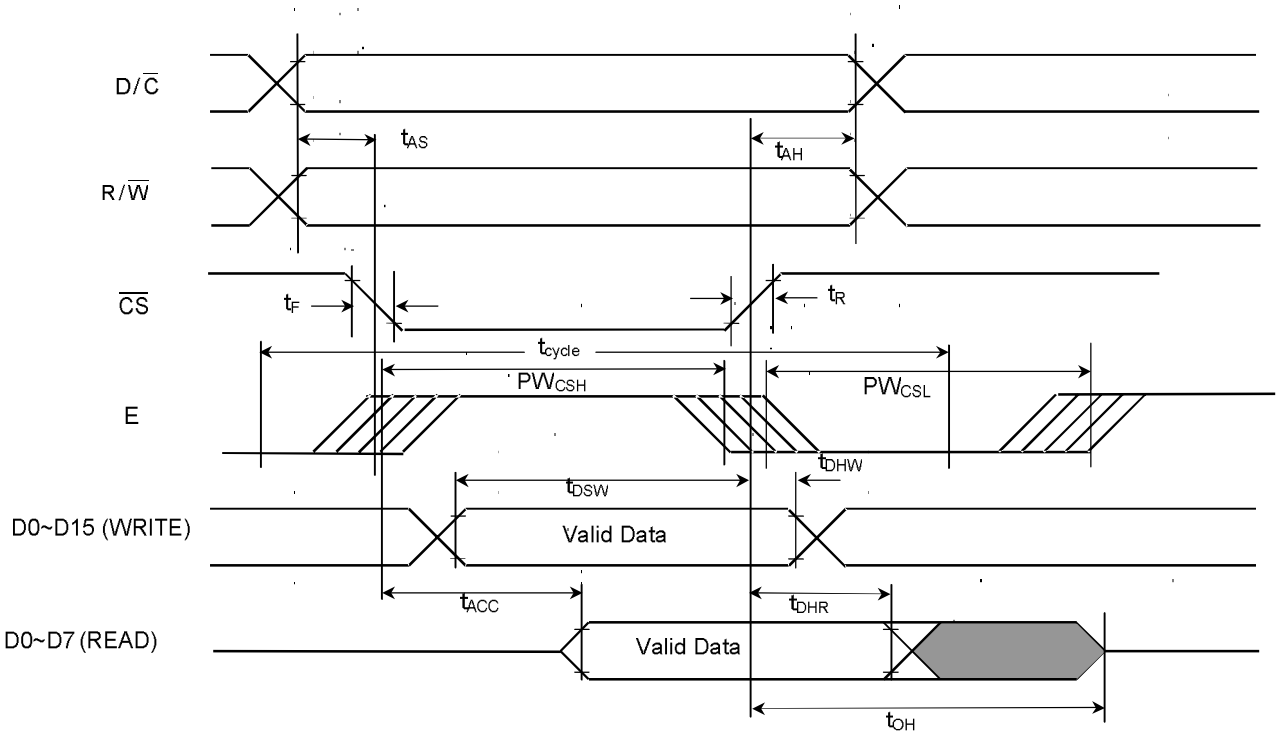
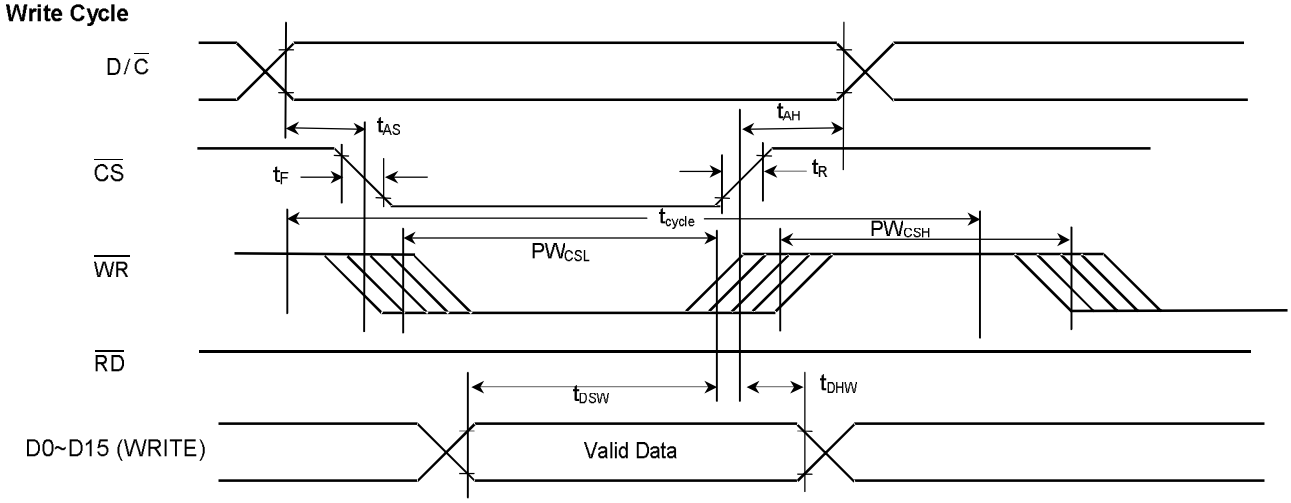


Figure 19 - 8-bit/16-bit Parallel 6800-series Interface Timing Characteristics

Table 20 - Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	250	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns
PW_{CSH}	Chip Select High Pulse Width (write cycle)	125	-	-	ns
PW_{CSL}	Chip Select Low Pulse Width (write cycle)	125	-	-	ns

Write Cycle



Read Cycle

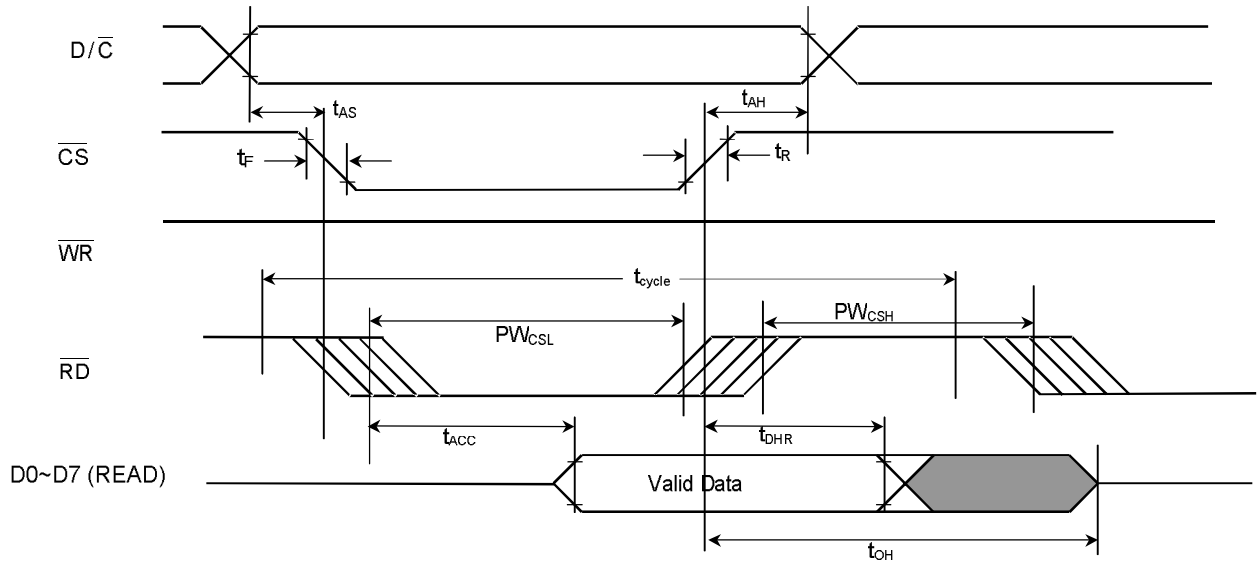


Figure 20 - 8-bit/16-bit Parallel 8080-series Interface Timing Characteristics

Table 21 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	66	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

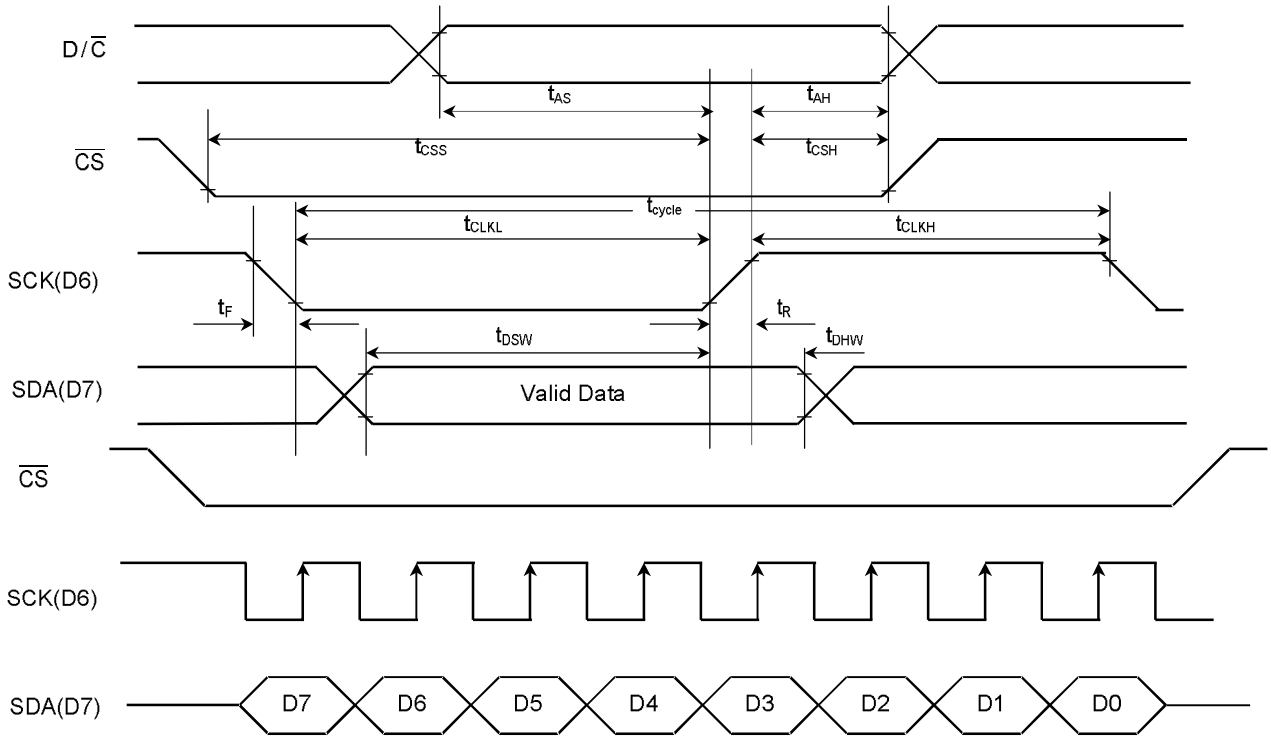


Figure 21 - 4 wire Serial Timing Characteristics (PS2=PS1=PS0=L)

Table 22 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	66	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

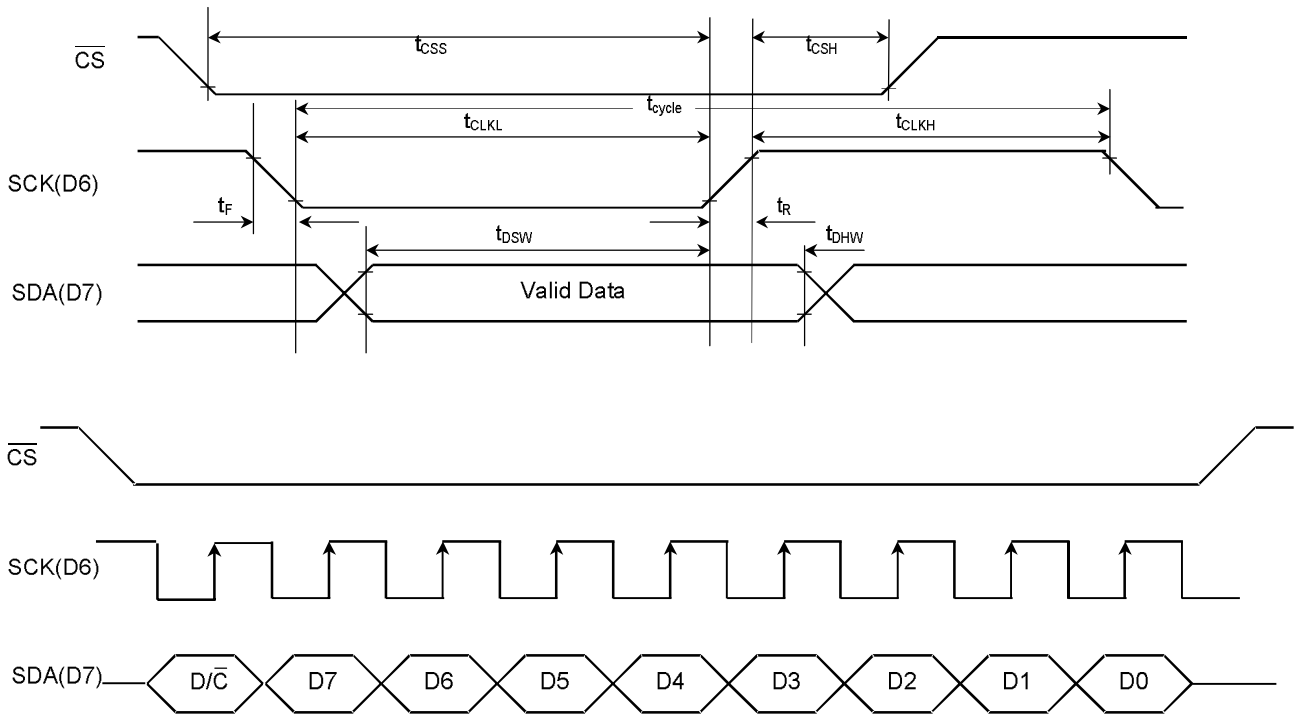


Figure 22 - 3 wire Serial Timing Characteristics (PS2=PS1=L, PS0=H)

Table 23 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	10	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

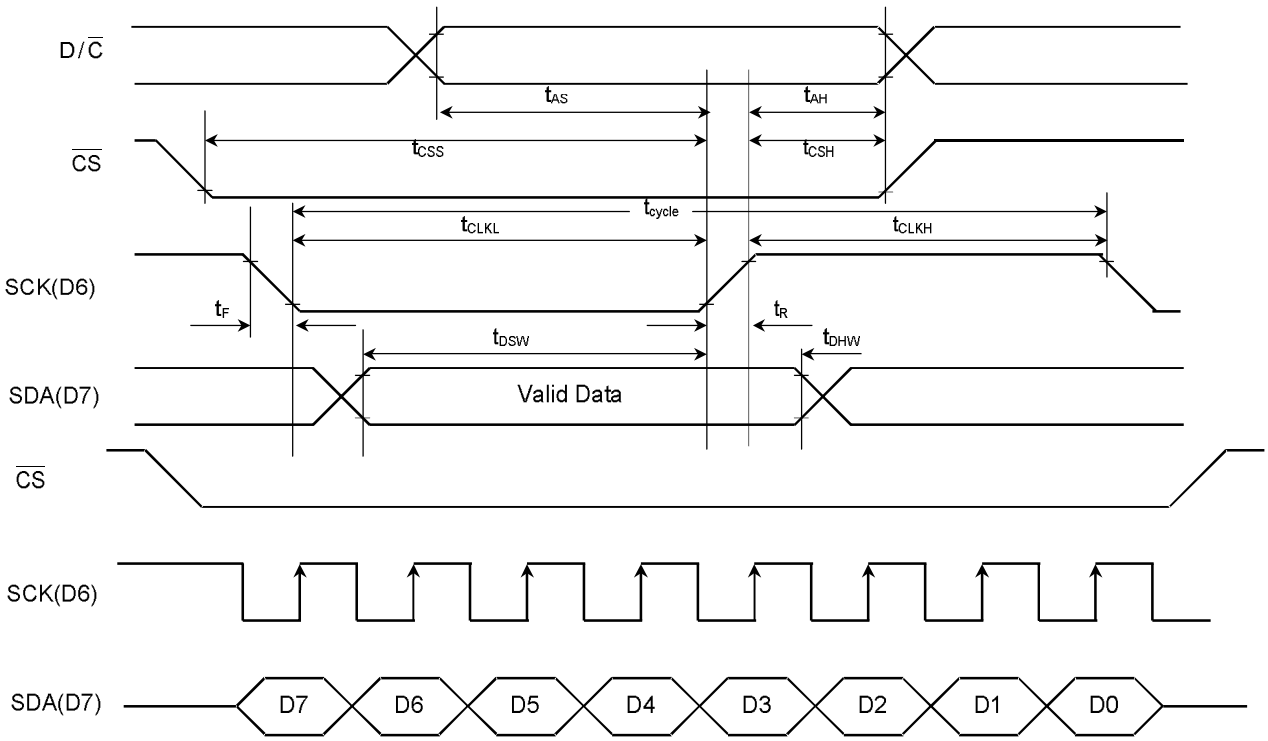


Figure 23 - 4 wire Serial Timing Characteristics (PS2=PS1=PS0=L)

Table 24 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	10	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns

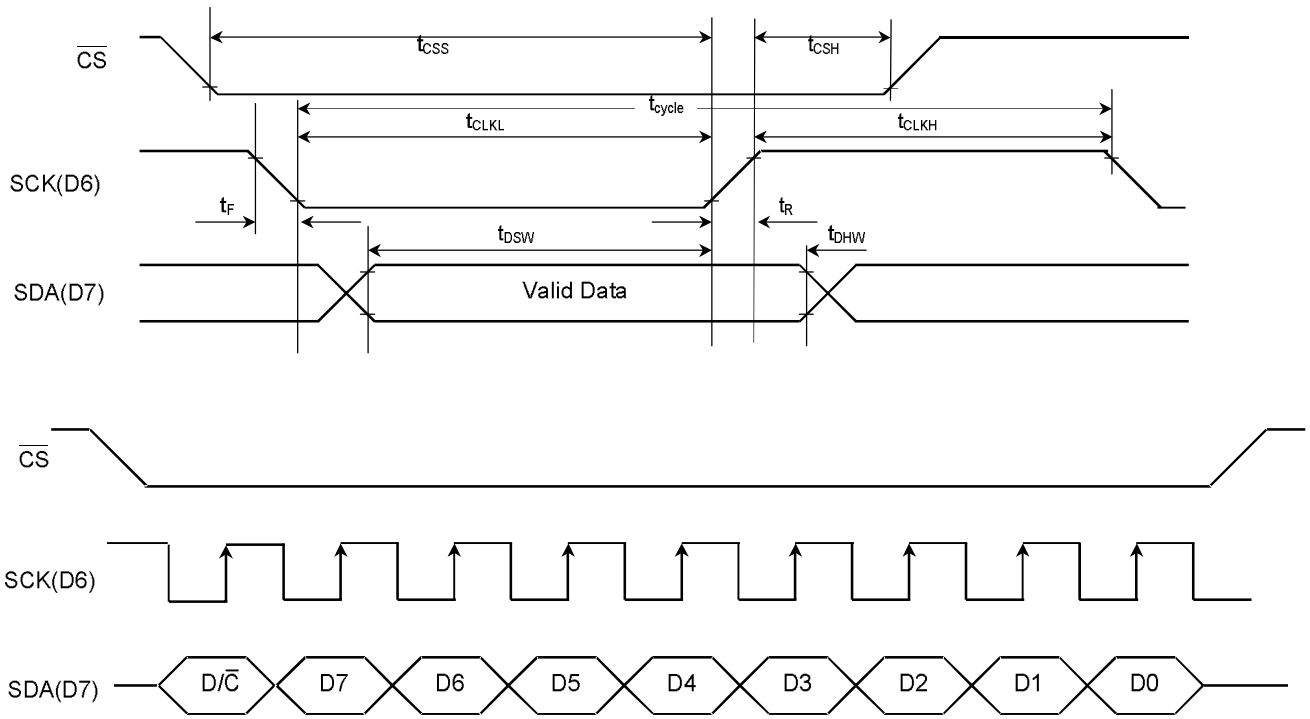
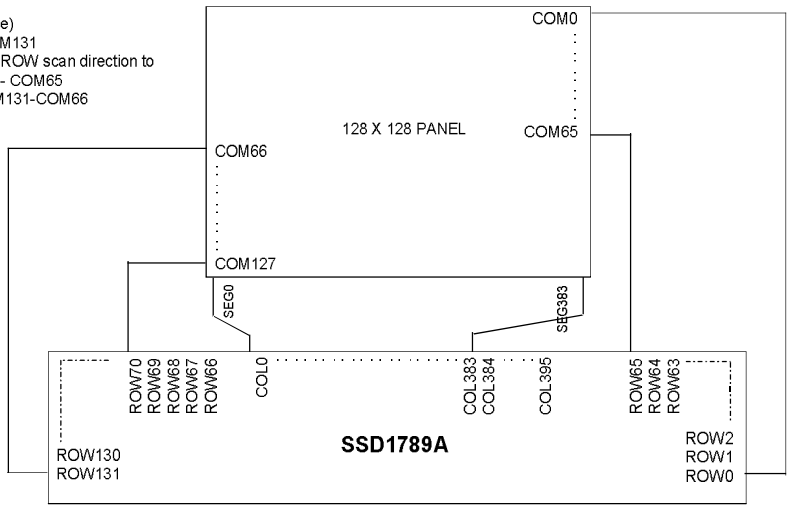
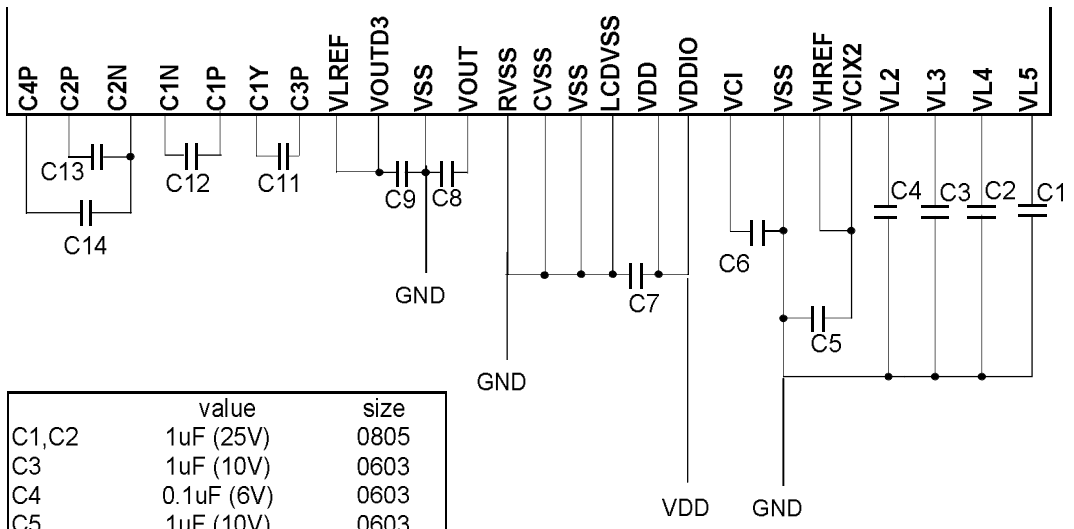


Figure 24 - 3 wire Serial Timing Characteristics (PS2=PS1=L, PS0=H)

13 APPLICATION EXAMPLES

COM/SEG connection of SSD1789A on 128x128 application:
Note:
1.write ram to page 0 to 127 (128 page)
2. use COM0 - COM65, COM70 - COM131
3.issue command (C)BB-(D)01 to set ROW scan direction to
ROW0-ROW65 -> COM0 - COM65
ROW66-ROW131 -> COM131-COM66

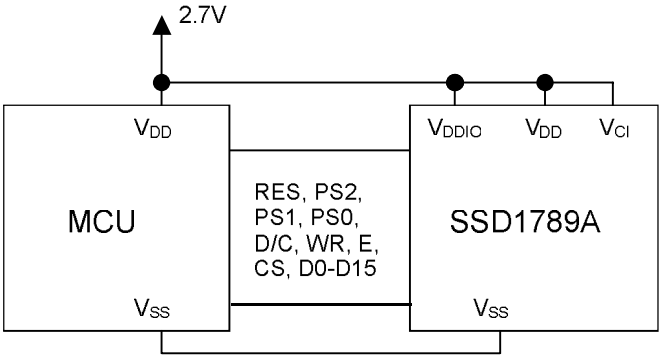




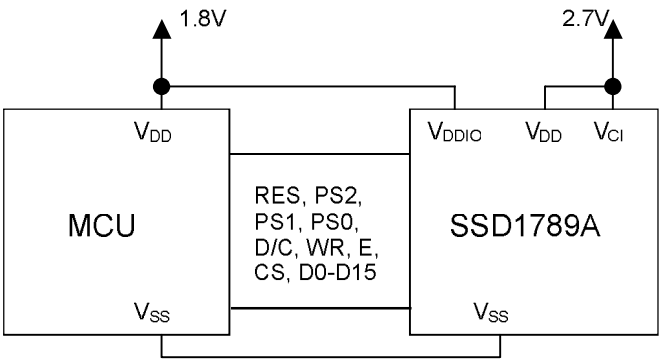
	value	size
C1,C2	1uF (25V)	0805
C3	1uF (10V)	0603
C4	0.1uF (6V)	0603
C5	1uF (10V)	0603
C6,C7	1uF (6V)	0603
C8*	4.7uF (25V)	1206
C9	1uF (25V)	0805
C11,C12	1uF (25V)	0805
C13,C14	1uF (25V)	0805

Figure 25 - Application example

Figure 26 - V_{DD}, V_{DDIO}, V_{CI} connection example

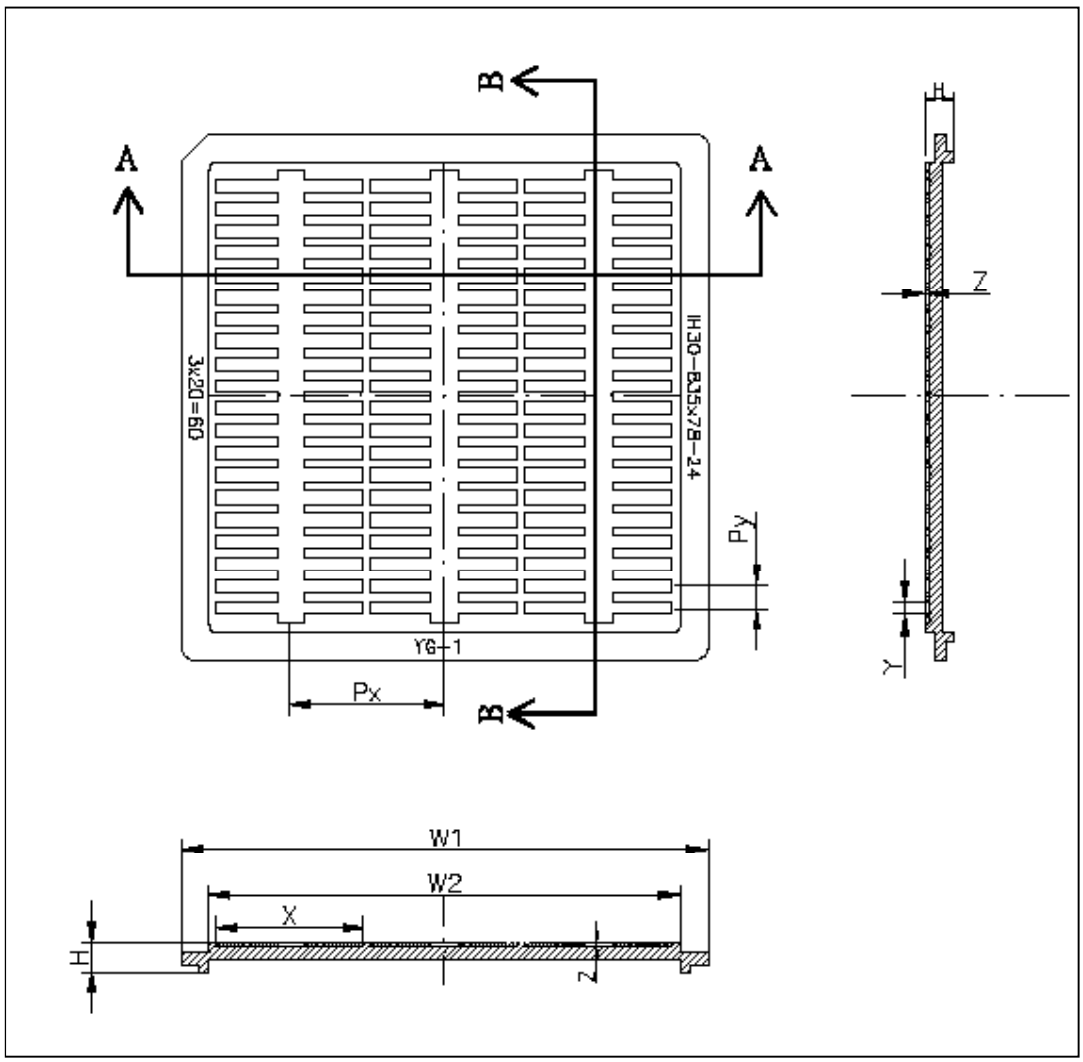


a)Normal Application;
V_{DD}=V_{DDIO}=V_{CI} =V_{DD}(MCU) =2.7V



b) Low Voltage MCU;
V_{DD} =V_{CI} =2.7V, V_{DDIO} =V_{DD}(MCU)=1.8V

14 SSD1789AZ DIE TRAY DIMENSIONS



Spec	mm	(mil)
W1	$76.0^{+0.2}/_{-0.1}$	(2992)
W2	$68.0^{+0.2}/_{-0.1}$	(2677)
H	4.2060.1	(165)
Px	22.3060.1	(878)
Py	3.2160.1	(126)
X	$21.20^{+0.1}/_{-0}$	(835)
Y	$1.98^{+0.1}/_{-0}$	(78)
Z	0.6260.05	(24)
N	60	

Figure 27 - SSD1789AZ Die Tray Dimension